Ultrasound Diagnostic Scanner

Model EUB-5500

TECHNICAL GUIDE

--- Principle of Operation ---

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L1E-EA0229-1

CONTENTS

Section 1 Introduction

1.1 Product Overview

Overview

EUB-5500 is a compact ultrasound scanner with multiple functions equipped with Doppler, color flow mapping function and so on, which circuits related to image quality are totally digitalized. It can be connected with phased array probes as well as linear and convex probes, and applicable to any type of use.

Also, it is fully equipped with various functions such as cine memory, cardiac function measurement, patient report function and so on. In addition, EUB-5500 runs on WindowsXP allowing it to be easily connected with various interfaces such as DICOM3.0 and so on.

Features

(1) True Digital Architecture

All sorts of ultrasound image processing for not only the beam former as a crucial point of image quality but also all mode of B, M, DOP, CFM and CFA are totally digitalized, and they are controlled by software.

(2) Improved resolution

Weighting of transmission and reception waves together with digital processing mentioned above realizes high spatial resolution, wide dynamic range and high contrast resolution.

(3) Improved color frame rate and image quality

Parallel beam and latest image processing technologies realize the Quadra beam process of color image. It achieves substantial improvement of frame rate compared with conventional techniques, as well as provides color images with high definition and high resolution.

(4) Applicable to multiple uses

Not only linear and convex probes but also phased array probes can be connected. Thus it is applicable to uses from abdomen and obstetrics to circulatory organ.

(5) Non-interlaced monitor as a standard

The RGB non-interlaced monitor adopted allows clear images without flickering to be viewed.

(6) WindowsXP is adopted as an OS.

WindowsXP is adopted for the operating system (OS). It allows DICOM3.0 and various interfaces to be easily connected.

(7) Easy-to-use keyboard

Key layout considering frequency of uses improves operability.

1.2 System Specification

1. Probe

   (1) Convex type : 2.0 ~ 10MHz
   (2) Linear type : 2.5 ~ 13MHz
   (3) Phased array type : 2.0 ~ 7.5MHz

2. Image examination mode

   (1) Standard configuration : B, B/B, B/M, M
   : B/PW, PW, CW, B/CW, CFM-B/CW,
   : CFM-B, CFM-B/CFM-B, CFM-B/CFM-M, CFM-M, CFM-B/PW,
   (2)Biplane probe connected : Real time B/B (Real time biplane)

NOTE: Refer to Instruction Manual for details

1.3 Environmental conditions

Observe the following environmental conditions for safe and correct operation of the equipment.

(1) Environmental conditions in operation

- Ambient temperature : +10°C～ +35°C
- Relative humidity : 30～85% (subject to no condensation)
- Atmospheric pressure : 700～1060hPa

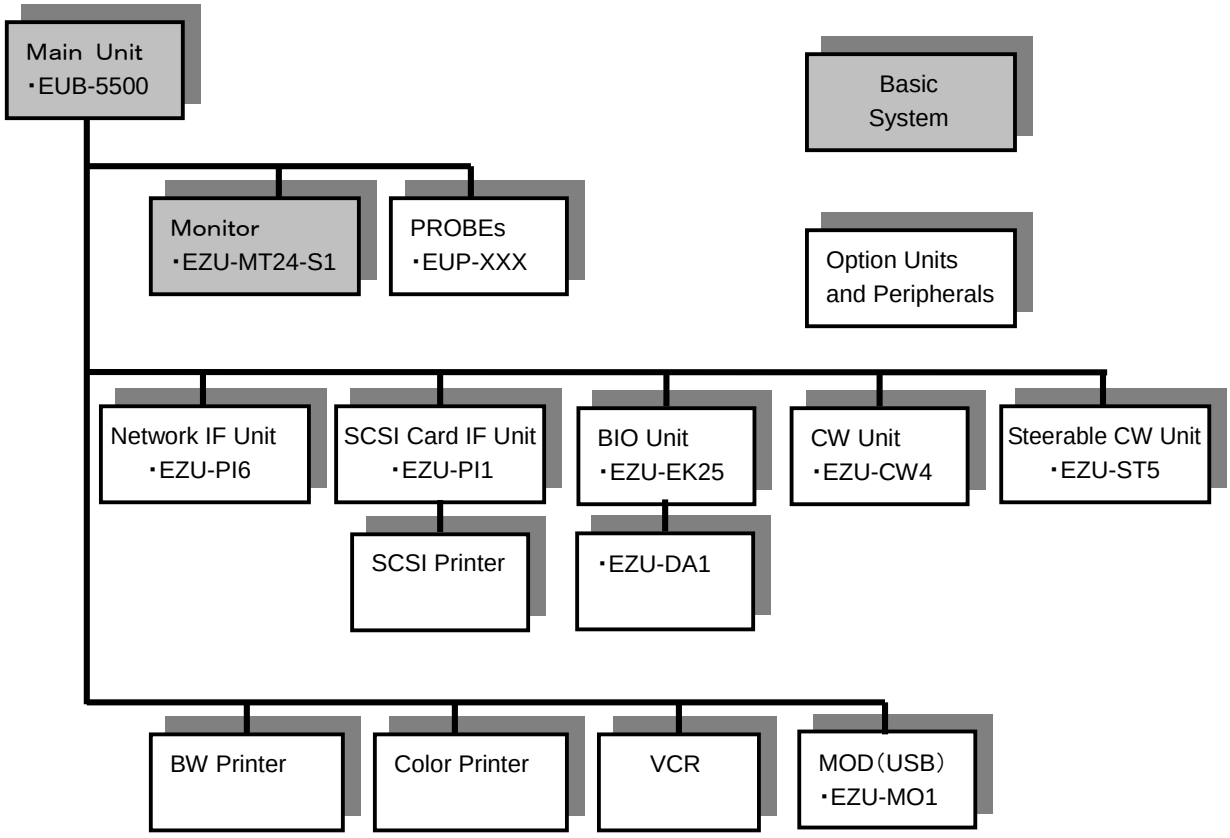
(2) Daily storage conditions

- Ambient temperature : -10°C～ +40°C
- Relative humidity : 10～90%(subject to no condensation)
- Atmospheric pressure : 700～1060hPa

(3) Environmental conditions for transportation (in packing)

- Ambient temperature : -10°C～ +60°C
- Relative humidity : 10～95%(subject to no condensation)
- Atmospheric pressure : 500～1060hPa

1.3 System Organization



NOTE: 1) ECG cable and electrodes are included in the BIO unit EZU-EK25.

2) Secure the peripheral devices to the equipment. If using the equipment without securing the peripheral devices, they may drop down due to vibration or inclination when moving the equipment.
For securing the peripheral devices, refer to TECHNICAL GUIDE (Installation).

1.4 Peripheral Device

Table 1.4-1 Recommended Peripheral Devices

Peripheral device	Manufacturer	Manufacturer's model, type	
		NTSC (EIA)*	PAL (CCIR)**
Black & white printer	SONY	UP-895MD	UP-895CE
	MITSUBISHI	P90U	P90E
		-	P91E
Color printer	SONY	UP-1800MD	UP-1800EPM
		-	UP-2800P/UP-2850P
		-	UP-2900MD/UP-2950MD
		UP-21MD	
	MITSUBISHI	CP700U	CP700E
		-	CP900E
		CP770DW with SB770(SCSI IF)	
	Polaroid (UK) Ltd.	-	TX1300SE
S-VHS VCR	SONY	SVO-9500MD	SVO-9500MDP
	PANASONIC	AG-MD835	AG-MD835E
	MITSUBISHI	HS-MD3000U	HS-MD3000E
Digital VCR	SONY	-	DSR-20MDP

* for the scaner unit of NTSC (EIA) TV display system

** for the scaner unit of PAL (CCIR) TV display system

NOTICE:

- These devices meet IEC60601-1 compliance.
- To use CP-770DW, EZU-PI1 is required.

Section 2 Safety

2.1 Classification of the Equipment

Classification of this ultrasound scanner by IEC60601-1 and UL2601-1 is as follows:

- Classification by type of protection against electric shock : Class I equipment
- Classification by grade of protection against electric shock : Type B and BF equipment (General requirements of medical equipment safety by IEC and UL)

2.2 Cautions in Operating the Equipment

(1) For maintenance inspection, refer to [Section 14 Maintenance and Checkup] of the Instruction Manual.

(2) In moving the equipment, refer to [Section 13 Movement] of the Instruction Manual.

(1) For starting up and shutting down the system, refer to the Instruction Manual [Chapter 4 Operation procedures].

2.3 Cautions in Maintaining the Equipment

(1) Do not use fuses other than rated.

(2) For rating of fuses, refer to labels and marks around the fuse holder.

(3) When removing PCB or connector, turn off ON/STANDBY switch and the breaker switch and wait more than 10 seconds before entering into the work.

(4) When adjusting the monitor, care should be taken for high voltage.

Table 2.3-1 Fuses of equipment

External Fuse	—	F1	3.15A/AC250V （AC100~120V） 6.3A/AC250V （AC220~240V）
		F2	1.6A / AC250V
Internal Fuse	Power Supply	F1 on Filter board in HM-071C	0.5A / AC250V
		F2 on Filter board in HM-071C	0.5A / AC250V
		F1 on Main converter AC/DC in HM-071C	6.3A / AC250V
		F2 on Main converter AC/DC in HM-071C	6.3A / AC250V
	Monitor	F100	3.0A / AC250V

2.4 Symbols

IEC establishes symbols to be used for the equipment. The following symbols are used outside and inside the equipment.


Protective earth (ground)


Equipotentiality


Attention, consult ACCOMPANYING DOCUMENTS


Off (power disconnection from the mains)

On (power connection to the mains)


TYPE B EQUIPMENT


TYPE BF EQUIPMENT


Dangerous voltage


Defibrillator-roof TYPE BF EQUIPMENT

Section 3 Operation

3.1 General Operation

Refer to the Instruction Manual.

3.2 Special Operation for Service Personnel

NOTE: 1) In the following sentences, “click” means placing the arrow pointer onto the object and pressing the ENTER key.

2) Operations described below are special ones exclusive for the service personnel. Be sure not to open to the users.

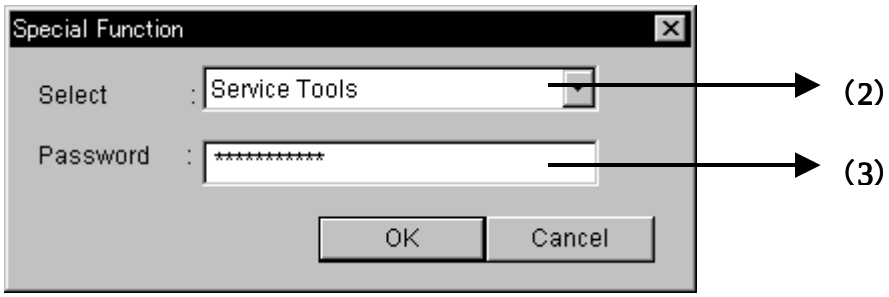
3.2.1 Initialization of system environment

(1) Press Ctrl + Alt + S key to display the “Special Function” dialog.

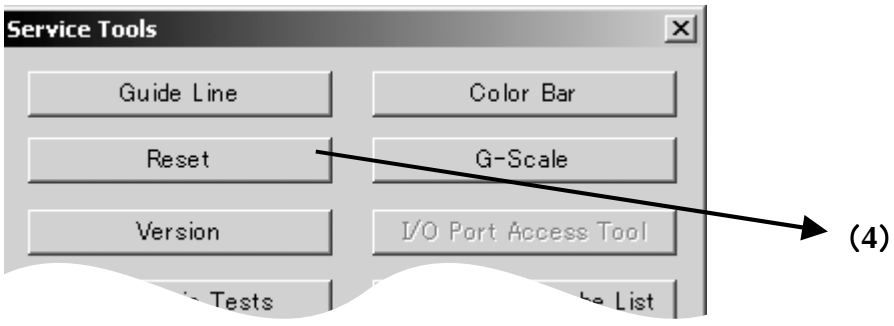
(2) Select “Service Tools” from the Select item.

(3) After entering “SERVICETOOL” for Password, click the “OK” button to start “Service Tools”.

NOTE: 3) For entering Password, make sure to type it in capital letters. (With the state of Caps Lock key located on the keyboard being lit in orange color.)

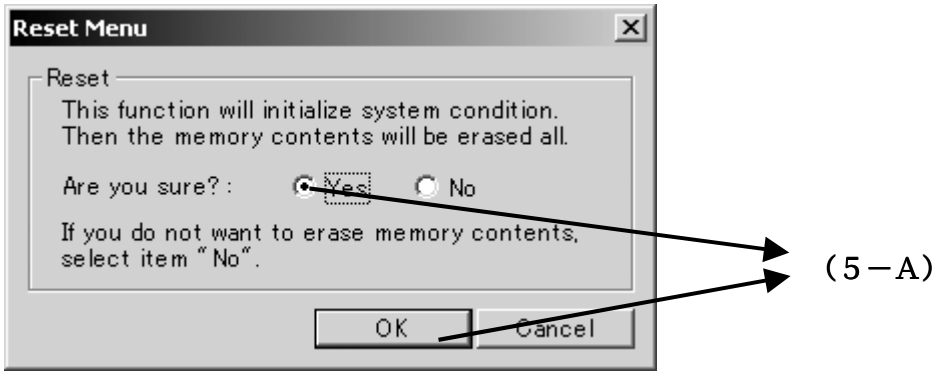


(4) Click the “Reset” button in “Service Tools”.



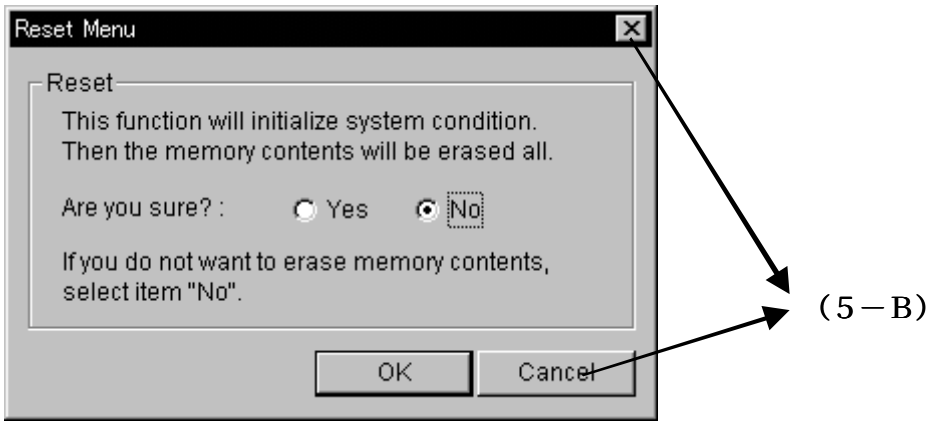
(5-A) If selecting “Yes” from “Reset Menu” and clicking the “OK” button, all the setup data is reset to those when shipped from the factory and the system is rebooted.

NOTE: Time data is retained.

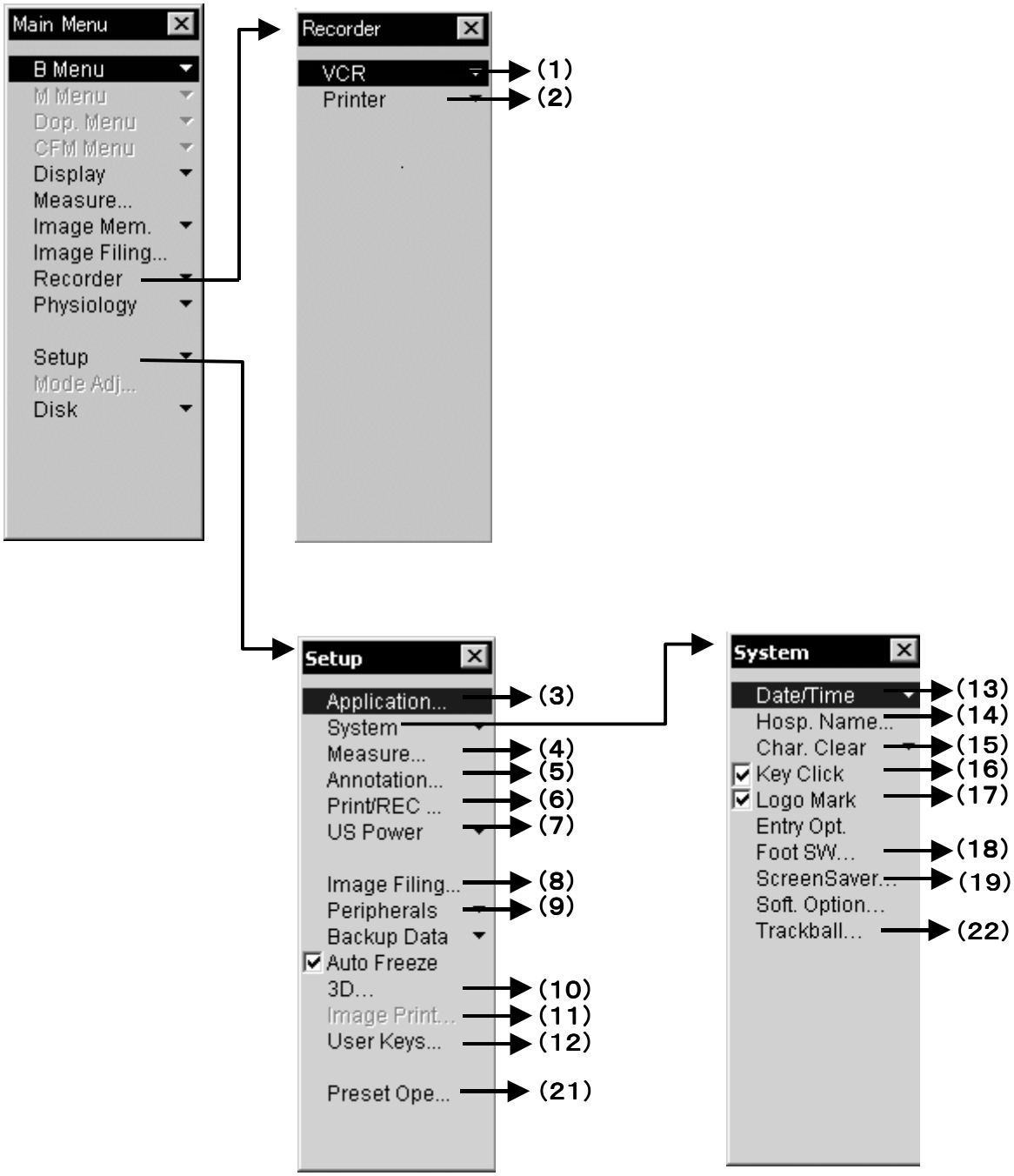


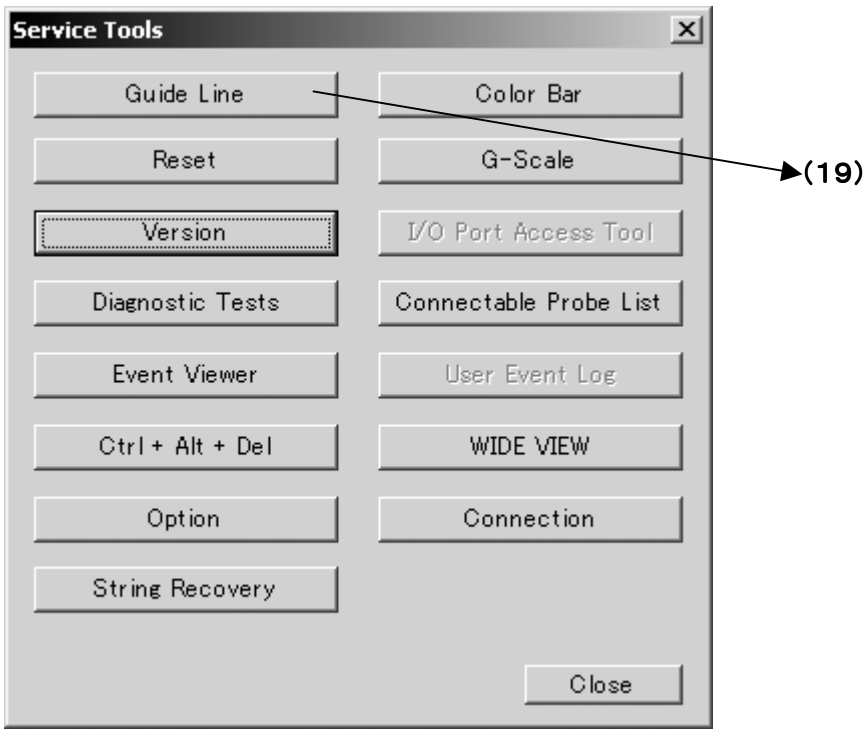
(5-B) If clicking “Cancel” or “Check box” (☒) in “Reset Menu”, “Reset Menu” ends and the process returns to “Service Tools”.

NOTICE：Don’t click OK button , where NO is chosen.



3.2.2 Contents of backup data





(1) VCR

VCRSelect the type of VCR to be connected.

(2) Printer
Select print time of the black/white video printer to be connected.

(3) Application
Set application data.

(4) Measure
Set a measurement method, measurement item and so on.

(5) Annotation
Register the hospital name.

(6) Print/REC
Select the recorder to be remotely controlled when clicking the print key and REC key.

(7) US Power
Select the initial value of US power when booting the system.

(8) Image Filing
Set data transfer related items.

(9) Peripherals
Set the connection related to the network and others.

(10) 3D
Set parameters to capture 3D images
(When EZU-3D4 or EZU3D2S is mounted.)

(11) Image Print
Set format for multi-screen printer output.

(12) User Keys
Set user defined function keys.

(13) Date/Time
Set clock data.

(14) Hosp. Name
Register hospital name.

(15) Char. Clear
Select automatic clearing comments entered onto the screen or not when freeze OFF and changing application.

(16) Key click
Select sounding a beep or not when clicking a key.

(17) Logo Mark
Select displaying characters of “HITACHI” at the upper left of screen or not.

(18) Foot SW
Select the foot SW.

(19) Screen Saver
Set the screen saver functions.

(20) Guide Line
Register any data to displayed for the puncture guide line.

(21) Preset Operation

Register any data to displayed for the BodyMark and Charavter

(22) Trackball Sensitivity

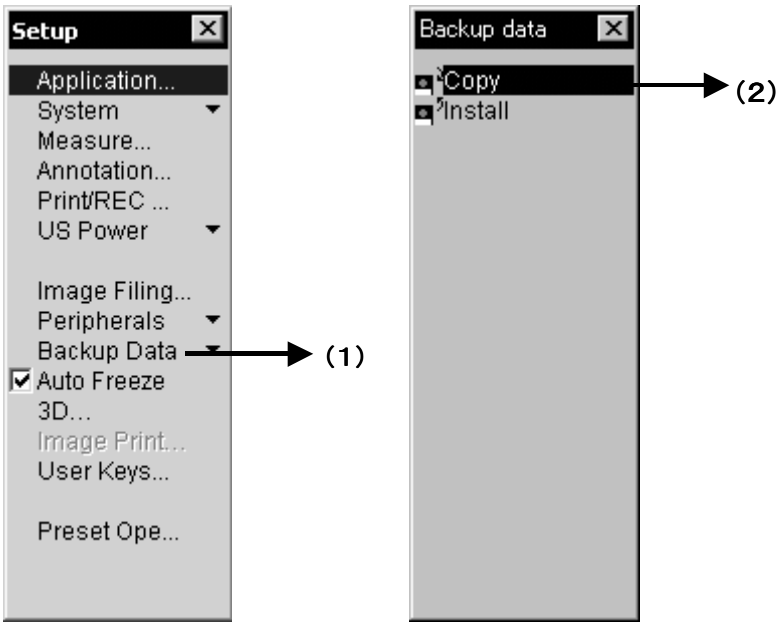
Register any data to set up a trackball sensitivity to every trackball priority

NOTICE: When version-up software, the backup data above is maintained. It is not reset to that when shipped from the factory.

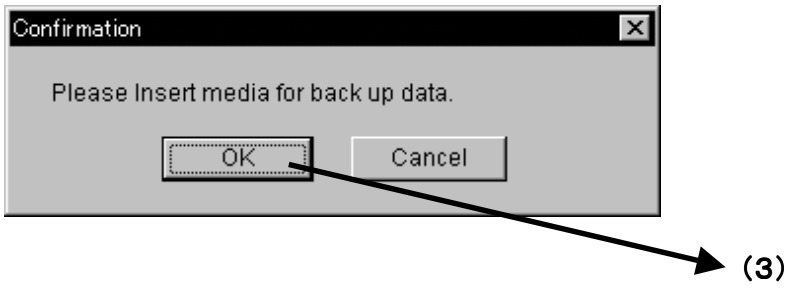
3.2.3 Saving backup data

(1) Select “Backup data” in “Setup” of “Main Menu”.

(2) Select “Copy” in “Backup data”.



(3) The following message appears. Set the CD-RW disk to the CD drive and click the “OK” button. This saves backup data and returns to “Backup data” menu display. Backup data is saved in the CD-RW disk as a folder titled “EUBBackup” in the CD-RW disk.



NOTE: Do not save backup data to CD-R. Use the CD-RW.

★ Error message when saving backup data ★

Displayed when the CD-RW disk is not prepared due to any of the following reasons:

- The CD-RW disk is not set to the CD drive.
- The CD-RW disk is write protected.
- The CD-RW disk has no sufficient free space.

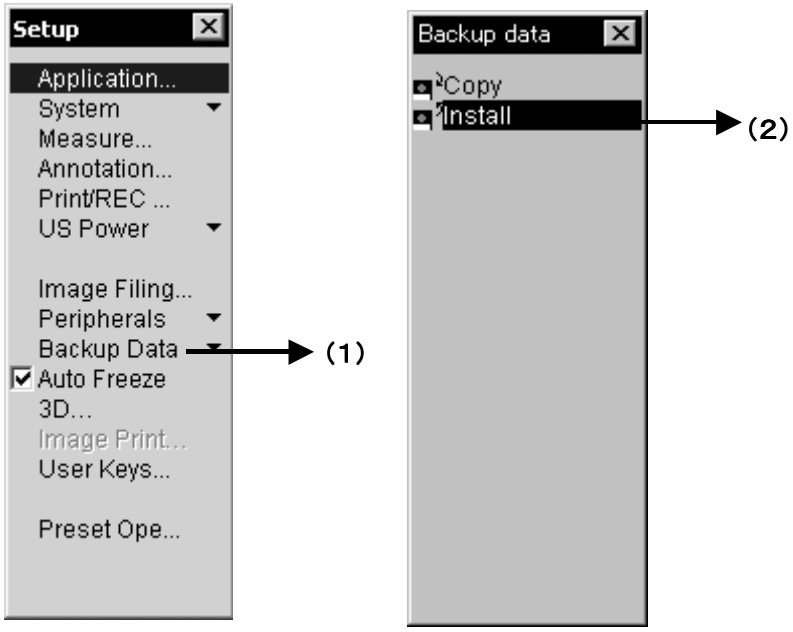
* Clicking the “OK” button returns to the “Backup data” menu.

3.2.4 Loading backup data

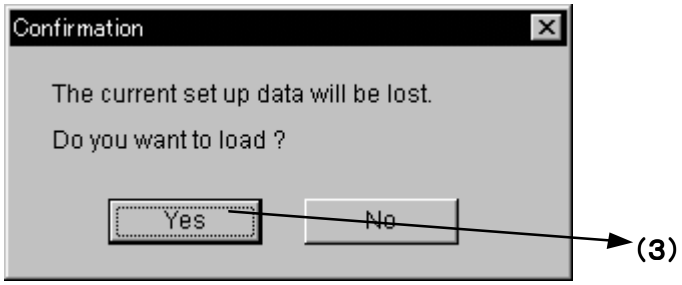
* Note that this operation deletes backup data saved in the system.

(1) Select “Backup data” in “Setup” of “Main Menu”.

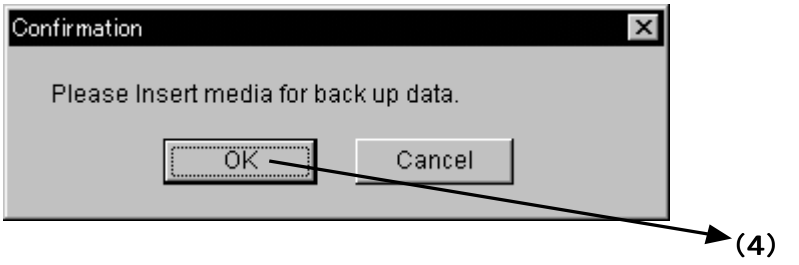
(2) Select “Install” in “Backup data”.



(3) The following message appears. If the backup data is to be installed, click the “Yes” button.



(4) The following message appears. Set the CD-RW containing the backup data to the CD drive and click the “OK” button. This installs the backup data and returns to “Backup data” menu display.



(5) Reading of backup data is performed, and equipment will be rebooted, if the O.K. button is clicked, since the message of the following figure is displayed after a while. Reading of backup data is an end after a reboot

Note: **This case has time in equipment starting depending on the contents of backup data. When backup data is read at the time of soft upgrade, time borrows from equipment starting 10 minutes to about 15 minutes.**

★ Error message when installing backup data ★

Displayedwhen the CD-RW disk is not prepared for backup data due to any of the following reasons:

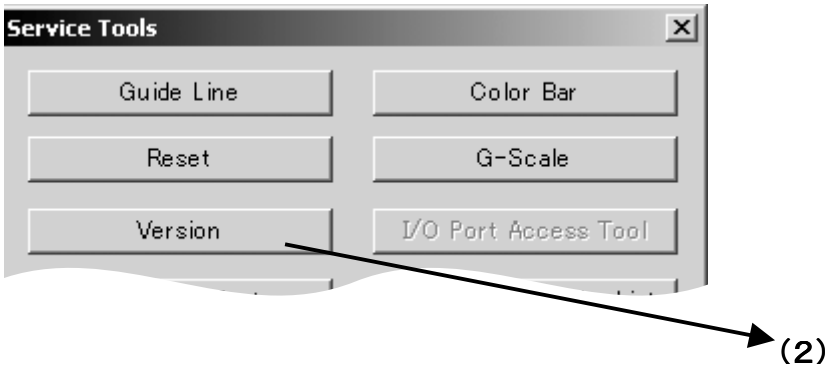
- The CD-RW disk is not set to CD drive.
- The CD-RW disk has no backup data.

* Clicking the “OK” button returns to the “Backup data” menu.

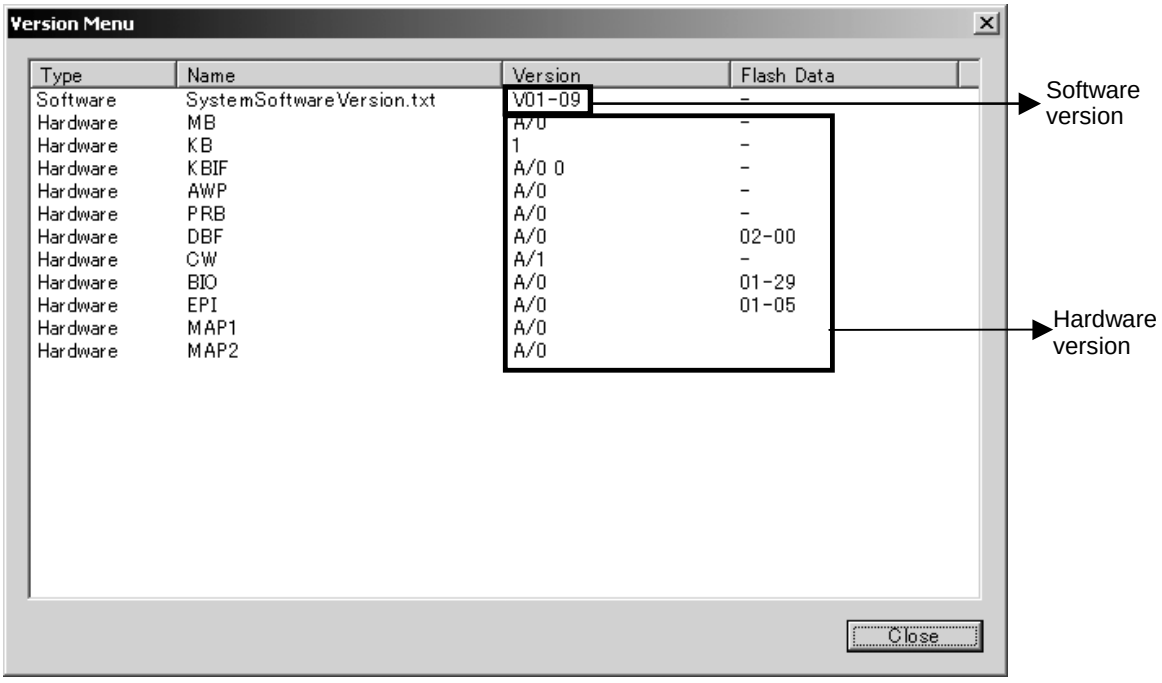
3.2.5 Displaying software and hardware versions

(1) Start “Service Tools”. Refer to 3.2.1 (1), (2) and (3).

(2) Click the “Version” button in “Service Tools”.



(3) Versions are displayed as shown below:



NOTE: “Not connected” in hardware version indicates no the board installed in the equipment.

3.2.6 Action be taken when the hard disk crashes

The followings describe an action to be taken when the hard disk crashes at the customer site.

3.2.6.1 Crash of HDD

Crash of HDD is divided into the following two cases:

1) Hardware crash: Ultrasound scanner does not start up because the HDD cannot be driven due to degradation of HDD hardware.

2) Software crash: The ultrasound scanner does not start because some file written in HDD is broken.

These two crashes may not be simply identified. Incase of HDD crash, take the action for hardware crash.

In either case, the action initializes user setting information. To prevent this initialization, it is helpful to use “Backup data” of “Main Menu” to backup user setting information periodically. By restoring this backup to the equipment after taking the action, user setting information can be protected (Refer to 3.2.3 and 3.2.4 for details).

The action to be taken in the two cases mentioned above will be described in the following subsections.

3.2.6.2 Preparation before the action

Prepare the following media supplemented to EUB-5500.

1) EUB-5500 System CD (CD-R)

Needs to start Recovery Medium and includes HDD recovery tools. Also, directly it can run the ultrasound scanner in place of HDD. Hereafter described as CD-R.

2) EUB-5500 Authentic Disk (FD)

Required when the system is provided with any onerous option.

Required for releasing protection of onerous optional functions.

Hereafter described as A-Disk.

A set of these media is supplemented to a system and exclusive to it. If these media supplemented to the system for which an action is to be taken cannot be prepared, stop HDD recovery.

NOTE: If using any media of the other system, the unauthorized copy protection function makes the media unusable after that.

3.2.6.3 Action to be taken when software crashes

In case of a software crash, the system can be recovered by reinstalling the ultrasound scanner software. The time required is approximately 30 Minutes

Procedure to reinstall software..

Switch on the unit and insert System CD into the ultrasound scanner's

(1) During the boot phase. A white bar will appear on the screen indicating that the unit is booting from the System CD when displaying HITACHI Logo mark.

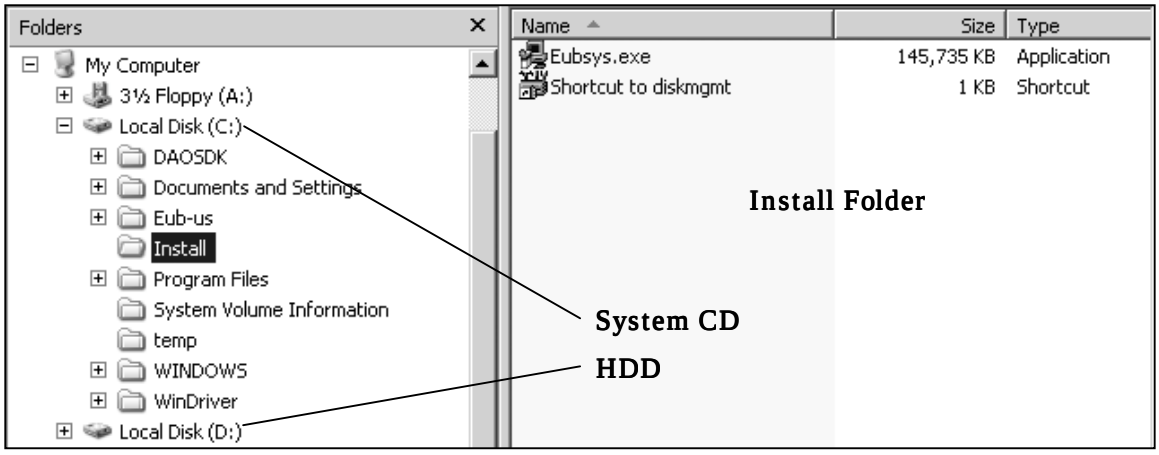
(2) When the start screen appears, (Approximately 5 Mins) depress "Ctrl + Alt + E" key

This operation needs to be executed just when the start screen is displayed. If not the e ultrasound scanner completes the boot up and displays the US image.. In such a case, turn OFF the system power and retry from the beginning.

NOTICE: The activation time of Explorer is long. Don't push "Ctrl + Alt + E" key frequently.

NOTICE: Except for case of invalidating STBY SW, don't turn off by breaker SW..

(3) Explorer of Windows XP Embedded is started (Approximately 2 Mins) and the file directory in System CD is displayed as below.



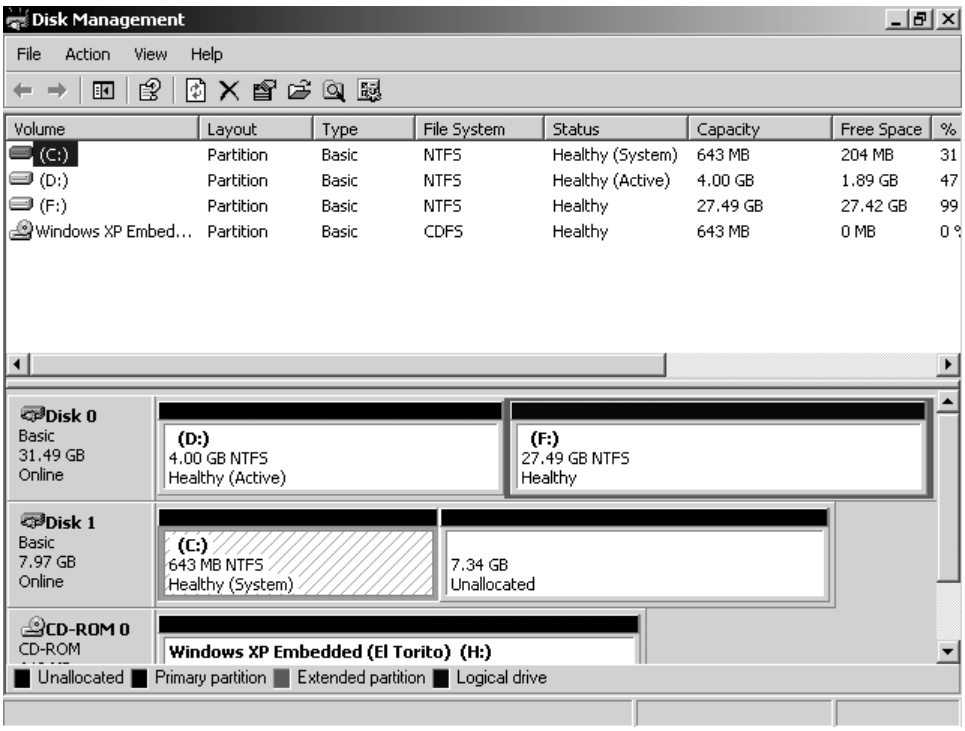
C drive: System CD: XP Embedded operating system and ultrasound program and Install program.

D drive: XP Embedded operating system, ultrasound program whitch is to be upgraded or repaired.

NOTICE : if system setting change is displayed , select the “No” and close the dialog.

(4) Open the “Install” folder on the CD and double click “shortcut of diskmgmt.exe” (C:/Install/diskmgmt.exe)

A dialog “Computer Management” appears.



(5)Check that the HDD is partitioned as below.

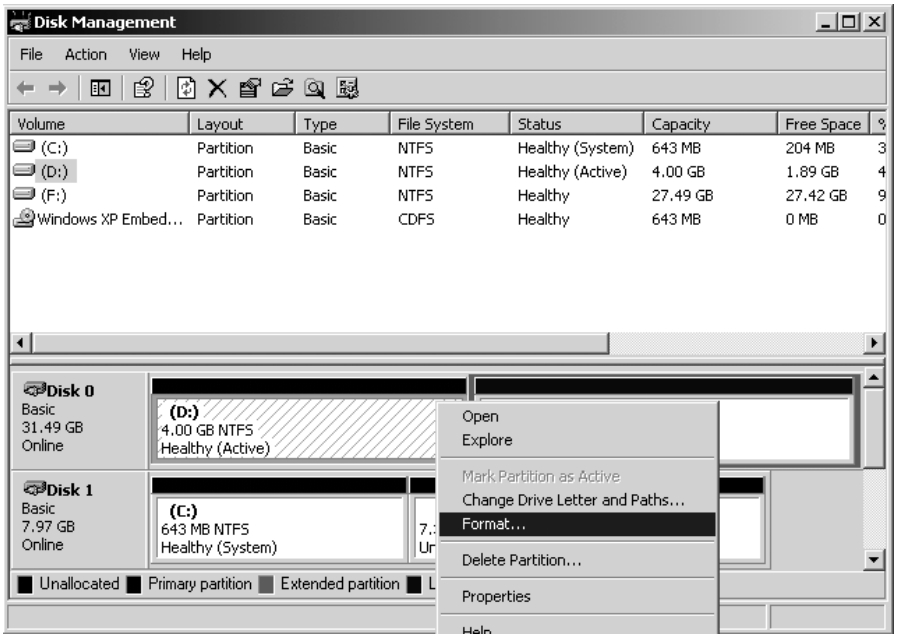
Partition 1: D = 4GB(4,096MB, and primary area) NTFS: (XP Embedded operating system and ultrasound program)

Partition 2: F = The other is expand Logical area NTFS: (Ultrasound work area)

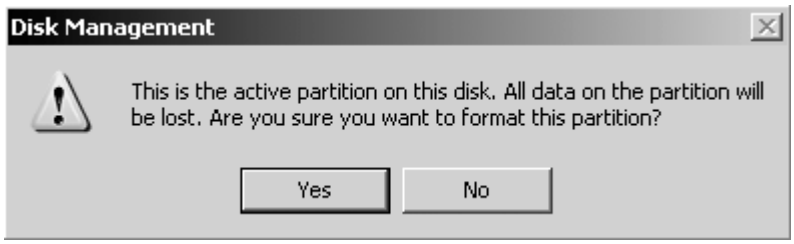
Format partition D drive and actives.

NOTICE: Do not format partition F, because included the user image data.

Close Disk manager.



(6) Press the “OK” button.



(7) Check below, and then press the “OK” button.

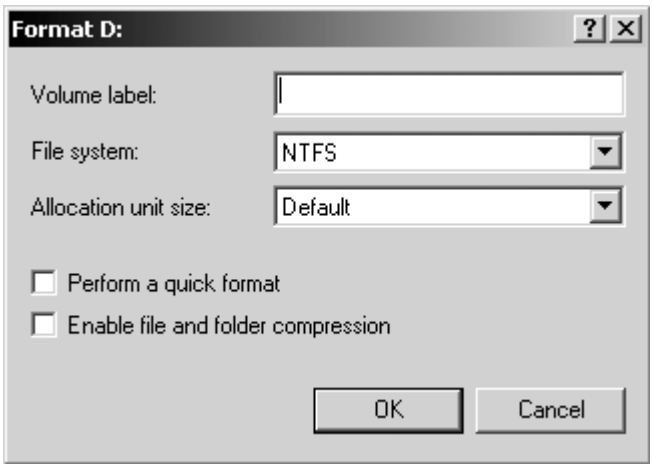
The file system is set the NTFS.

The Allocation unit size is set the Default

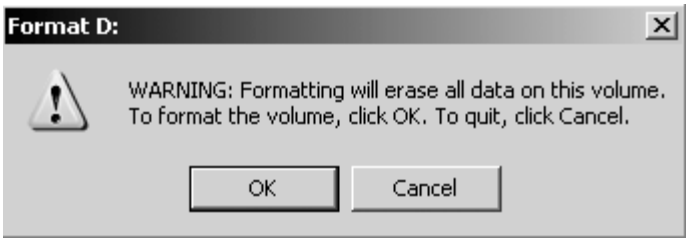
“Perform a quick format” is not checked. (There is no ✔ mark in check box)

“Enable and folder compression” is not checked. (There is no mark in check box)

Set the volume label to a blank.(refer to following photo)



(8) Click the “OK” button.

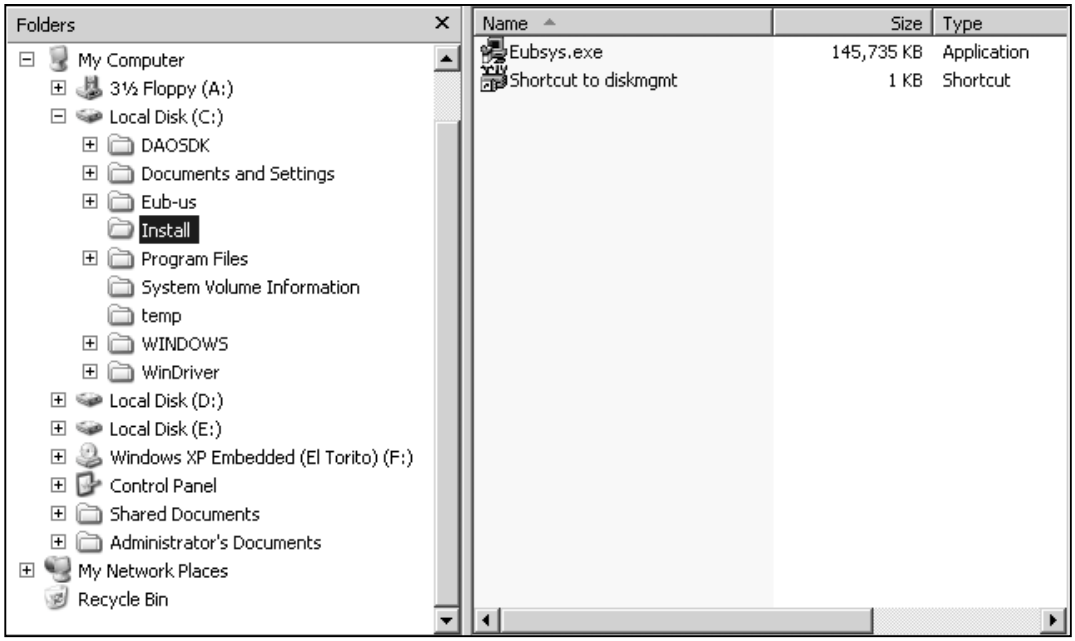


The progress is displayed on D drive in disk management.

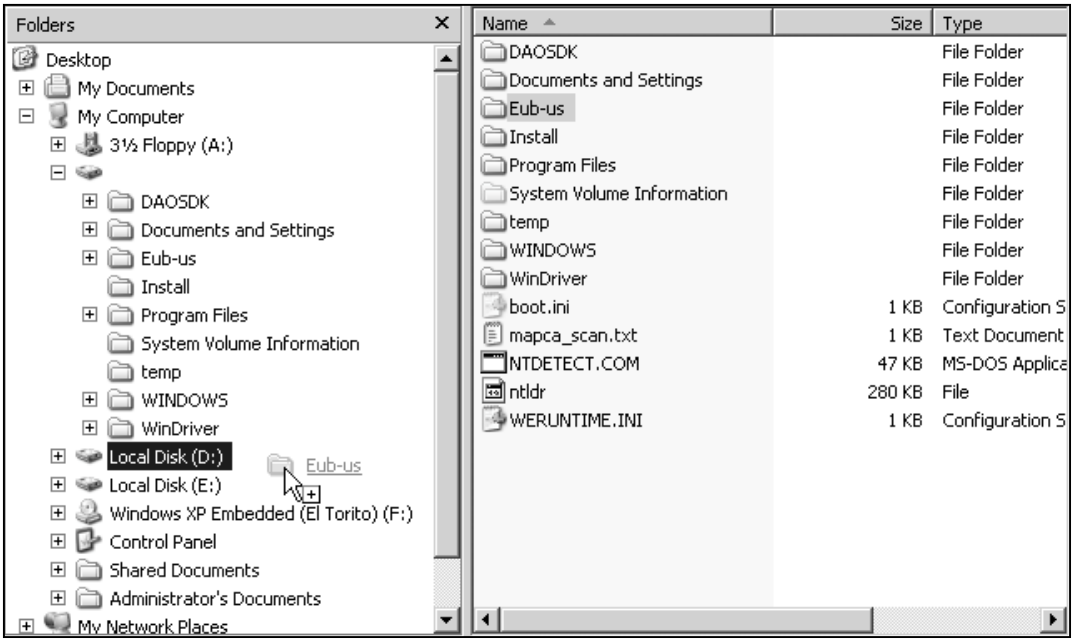
When progress reach the 100% , format is finished and drive status become “Active”

Click the ✕ in disk management. the disk management is closed after clicking.

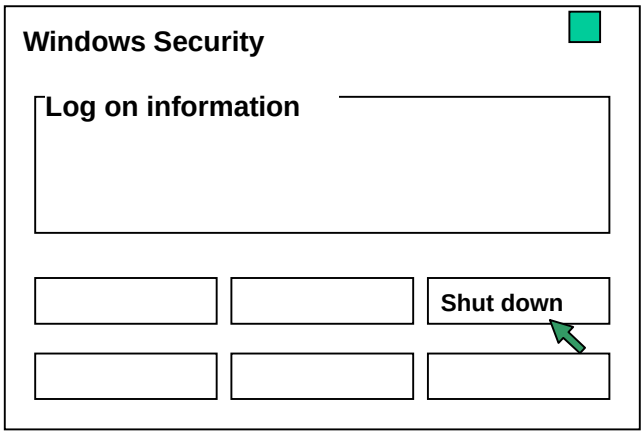
(9)Double click “EUBsys.exe” in Install folder, and then automatically create XP Embedded operating system image.



(10) Copy “Eub-us” folder from CD (C:/Install) to HDD partition D.



(11) Press “Ctrl + Alt + Del” and select “Shutdown”



(12) Select the “shut down” and click the OK button.

(13) Push the STBY SW after shutdown and start the system.
When BIOS logo appear on screen , push the eject button of CD drive.
And put out the CD media from CD drive . Close the tray of CD drive .
This operation needs to be executed just when the start screen is displayed. If not the ultrasound scanner completes the boot up and displays the US image. In such case, turn OFF the system power and retry from the beginning.

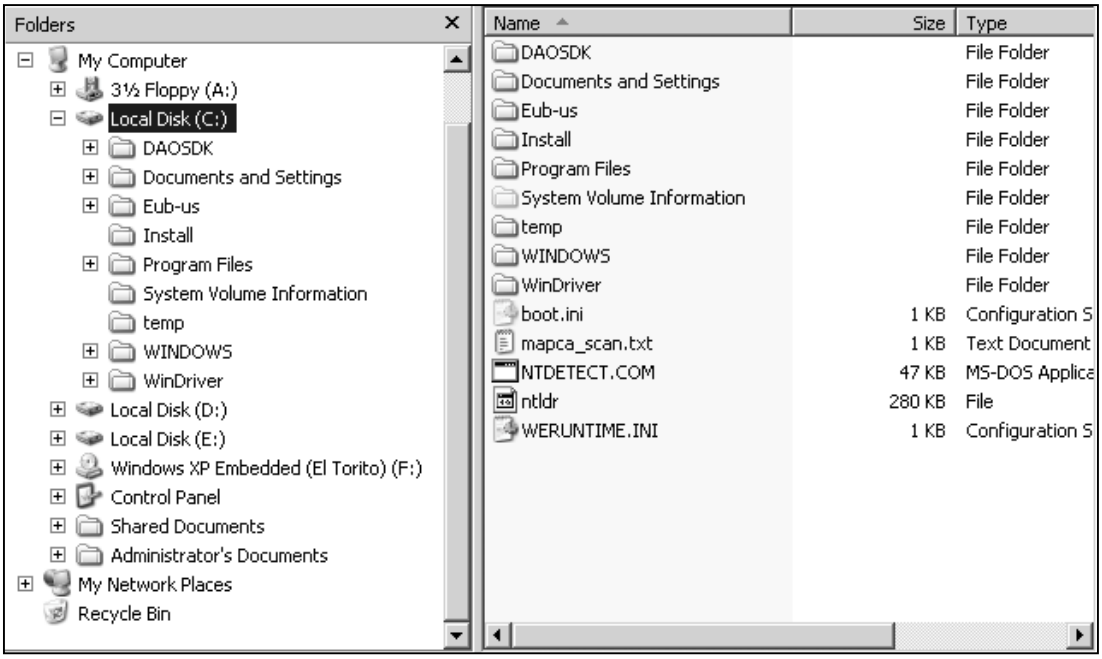
(14) When the start screen appears, (Approximately 5 Mins) depress “Ctrl + Alt + E” key

Explorer of Windows XP Embedded is started. (Approximately 2 Mins)

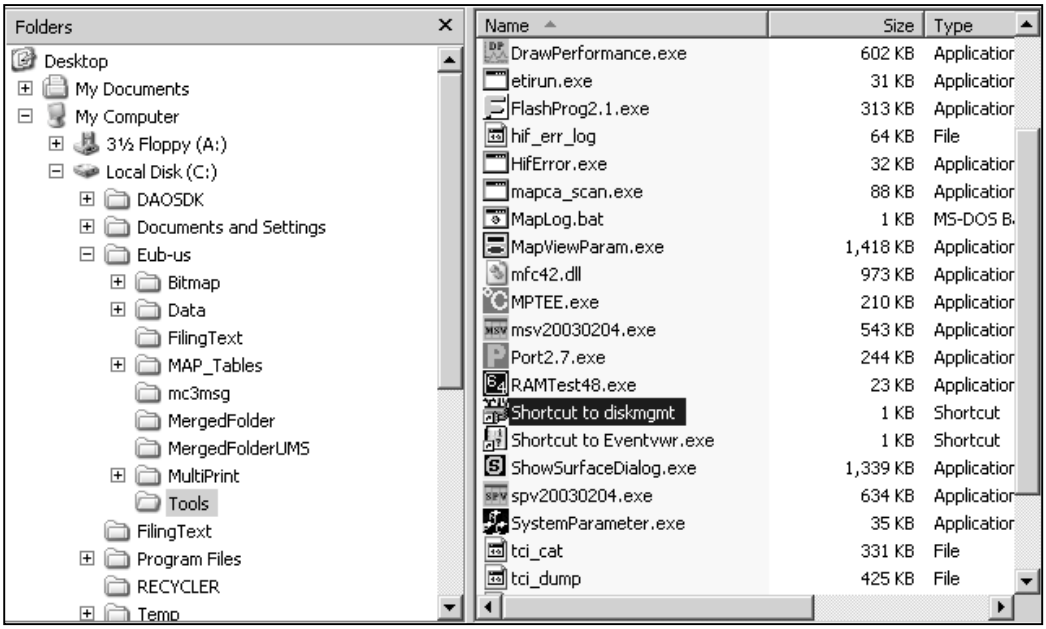
Check the drive letter of CD drive.

NOTICE: If it is not “H” , change the draive letter to “H”

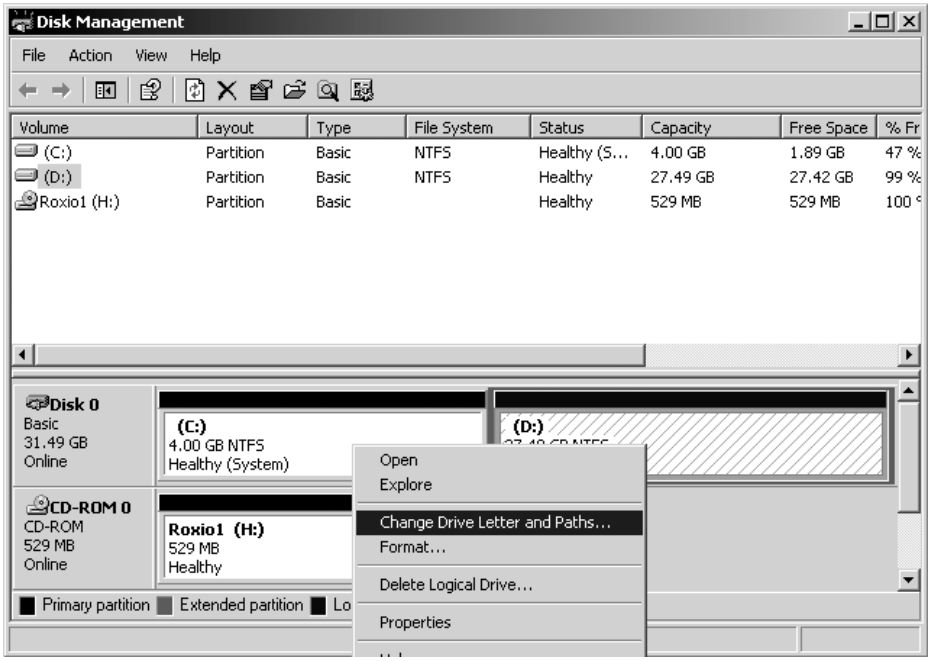
NOTICE: If system setting change is displayed ,select the “No” and close the dialog. .



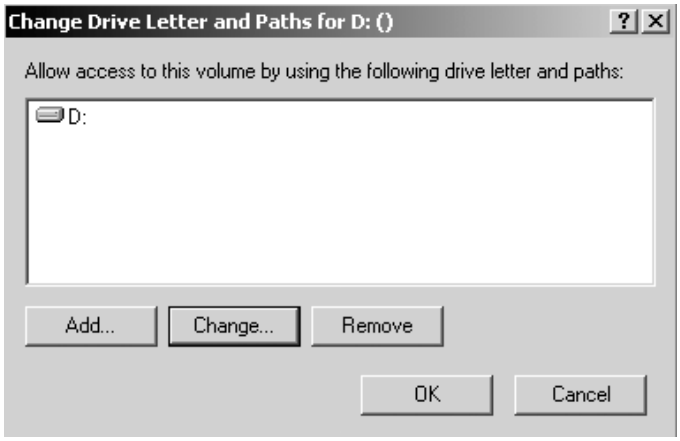
(15) Open the “C:/Eub-us/Tools” folder on the HDD partition and double click “shortcut of diskmgmt.exe” (C:/Eub-us/Tools/diskmgmt.exe)



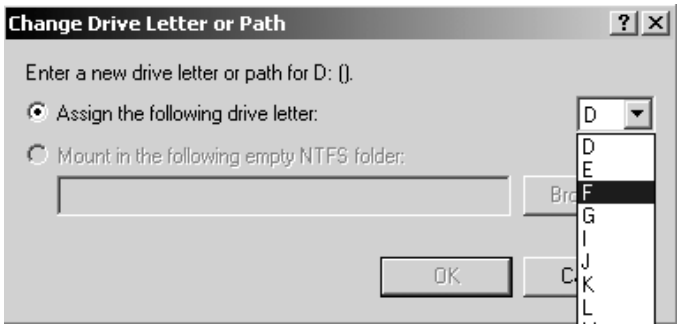
(16) Move the cursor to D drive on disk0 . press undo key and click the “Change drive letter and Paths..”.



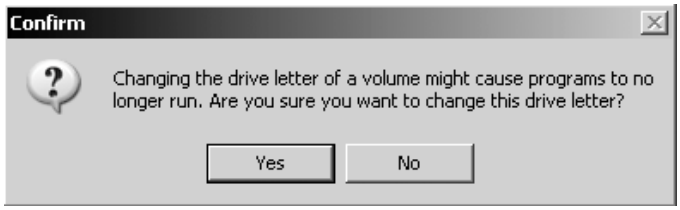
(17) Click the “Change “ button.



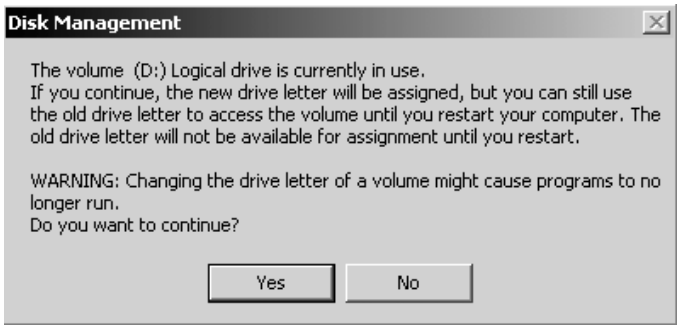
(18) Select the “F” from list and click the “OK” button



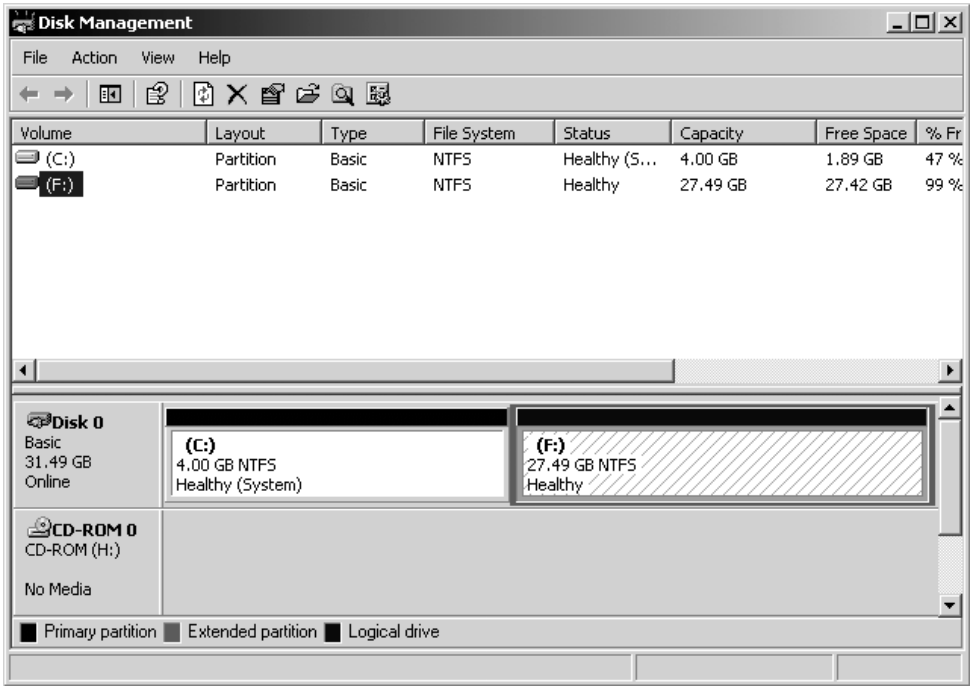
(19) Click the “Yes” button.



(20) Click the “Yes” button and continue assignment of drive.



(21)Confirm the drive letter is changed from D to F. Close the dialog by clicking ✕



(22) Shut down in accordance with (11)(12).

Procedure to repairing has been completed now. After this, the ultrasound scanner can be started as usual.

If option software(s) have been installed on the system, install them again referring to the option’s Technical Guide.

When the ultrasound scanner software in HDD is installed, protection is applied to onerous options. This protection needs to be released using A-Disk. For the method to release it, refer to Appendix A.

If following dialog is displayed during re-booting up , select the “Yes”.

3.2.6.4 Action to be taken when harddisk crashes

In case of Hard (HDD) crash, it is necessary to require the new HDD from factory and change it, and install all software to the HDD. It can be used the ultrasound system by attached System CD still sending the new HDD from factory. Refer to as followings:

The following describes a method to recover from software crash.

Procedure for starting the Ultrasound equipment from the System CD

1 Turn on the equipment.

2. Insert the System CD into the CD drive of the Ultrasound equipment during displaying the BIOS logo

3. The initial window appears and the Ultrasound equipment starts.

[1] Procedure of System CD

(1) Power on the ultrasound equipment.

(2) Immediately insert System CD into the ultrasound scanner's CD drive when displaying HITACHI Logo mark.

(3) Displaying ultrasound boot up image and start up the equipment.

Note1: In case of starting up System CD, it cannot be used the optional function (ex. SCSI printer, DICOM, Network, ODM and etc)

Note2: After starting up the ultrasound software, if displaying dialog of restart up or not for discovering new hardware, then select “no”.

[2] Procedure to install of the new HDD

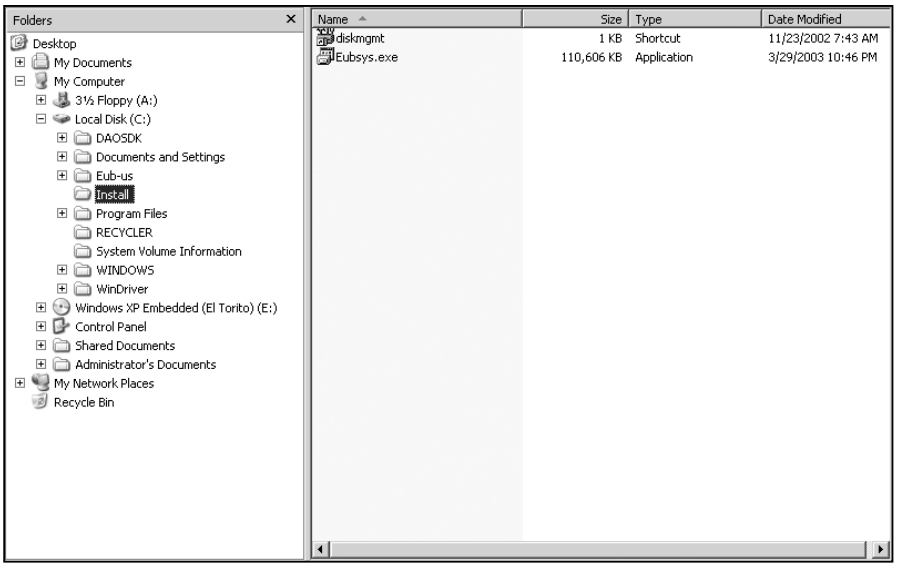
Note: In case of attached MO drive (optional EZU-MO1), take off the connector USB cable, and install as followings. After finished the install, the Drive letter of MO setting “D”. Power on the ultrasound equipment.

(1) Immediately insert System CD into the ultrasound scanner's CD drive when displaying HITACHI Logo mark.

(2) When the start screen appears, depress “Ctrl + Alt + E” key

Note: It is necessary to depress when displaying start screen. If not depress the key; repeat from (1) by standby switch, as it is finished start up the ultrasound software.

(3) Explorer of Windows XP Embedded is started and the file directory in System CD is displayed.

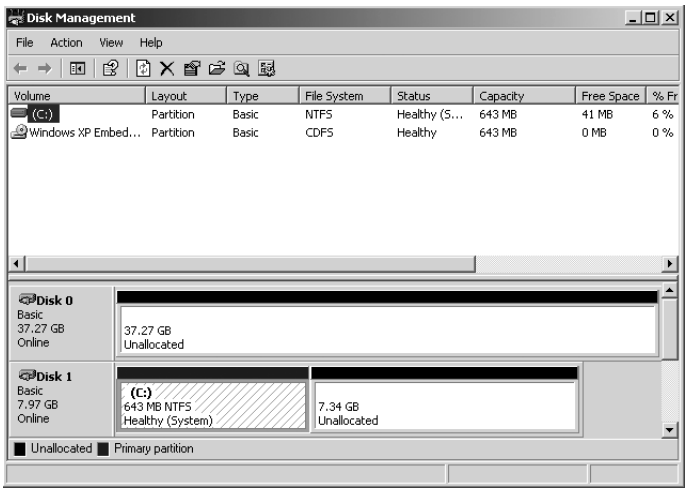


Note: If displaying dialog of restart up or not for new hardware, then select “no”.

(4) Open the “Install” folder from the file directory and double click “shortcut of diskmgmt.exe” (C:/Install/diskmgmt.exe)

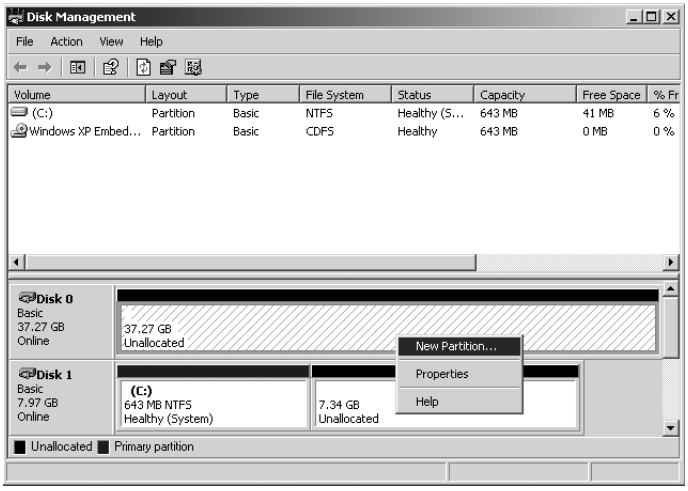
Note: As quite new HDD is sleep mode, if appeared the dialog of discovered new HDD, press repeating Next button and finish at last.

(5) A dialog “Computer Management” appears.

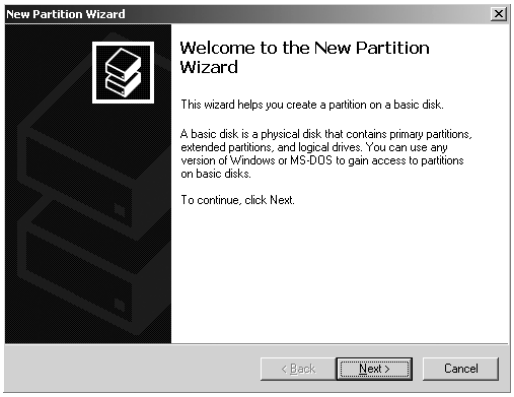


(6) Move cursor to Disk0 area and press UNDO key, then appear the followings dialog and select “New Partition...” and press ENTER key.

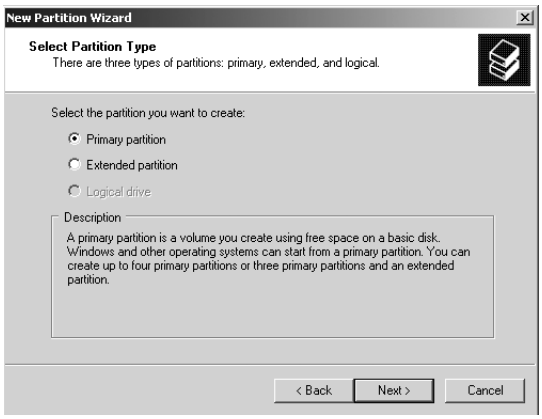
Note: Not recognized still making partition and logical drive.



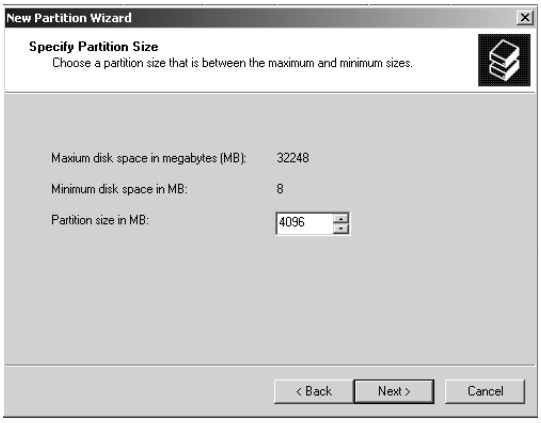
(7) Click “Next>” button.



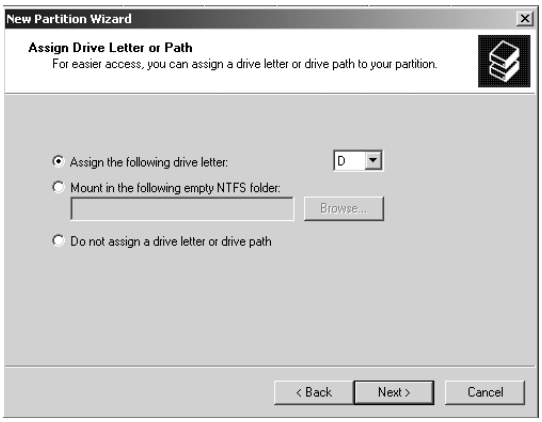
(8) Recognized item of “Primary partition” and click “Next>” button.



(9) Input “4096” (MB) for primary partition size and click “Next>” button.



(10) Recognized “D” for drive letter and click “Next>” button.

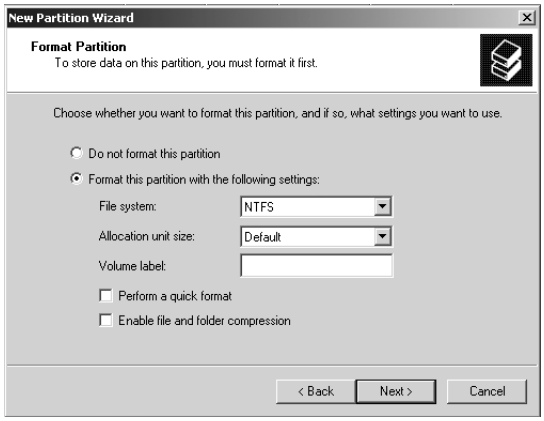


(11) Setting item as followings and click “Next>” button.

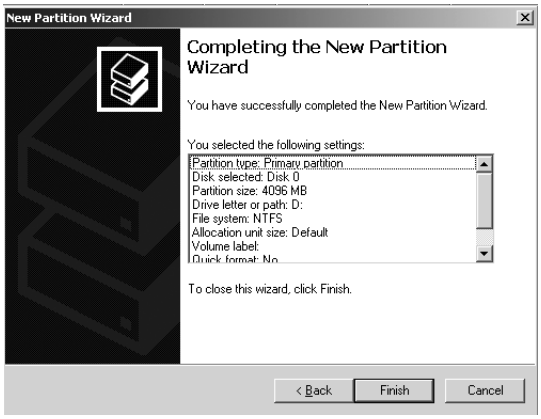
Set File system to NTFS.

Set allocation unit Default.

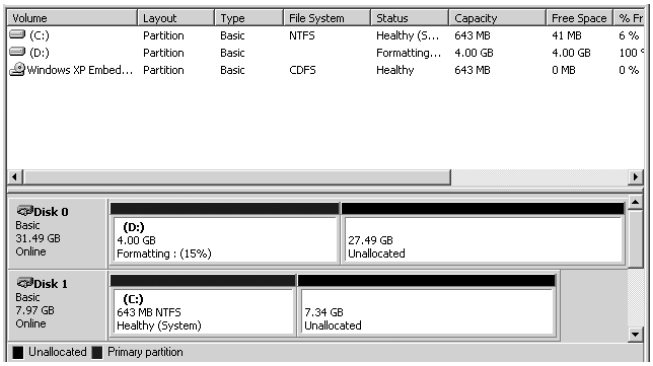
Set volume label to blank.



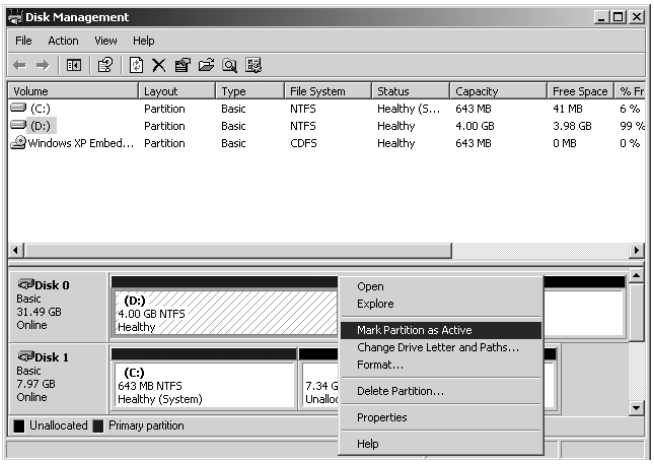
(12) Click “Finish” button.



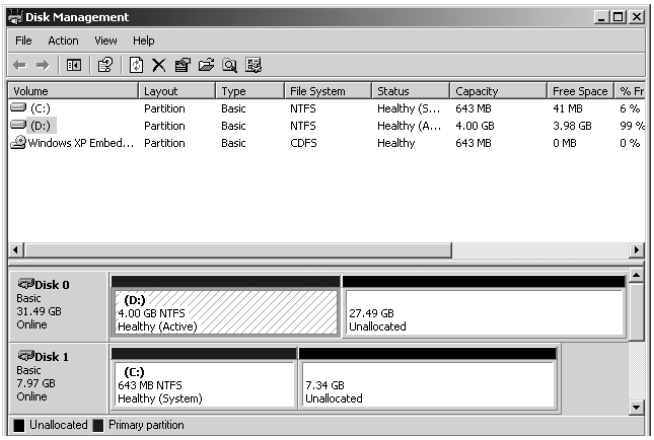
(13) Start D drive formatting and finish to 100%.



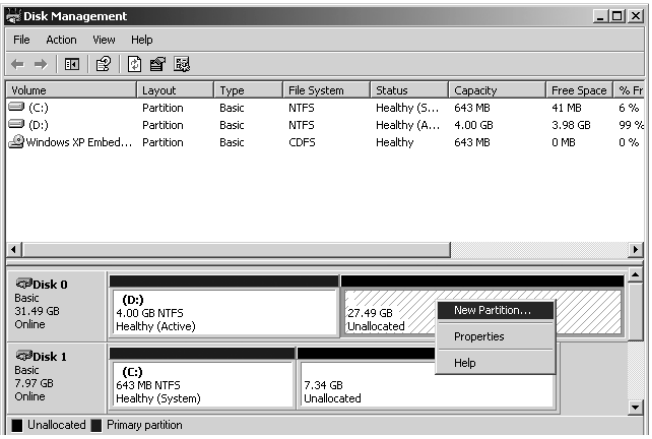
(14) Move cursor to D drive and press UNDO key, and select “Mark partition as Active” on menu.



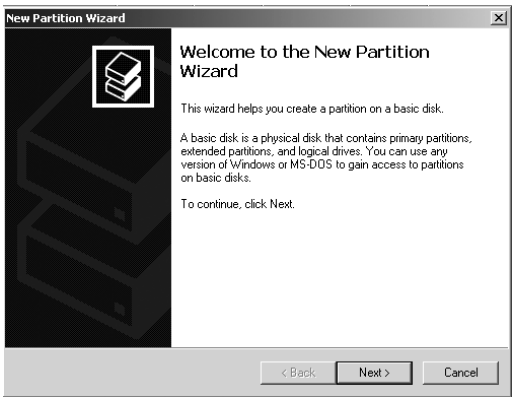
(15) Displaying “Active” mark to D drive.



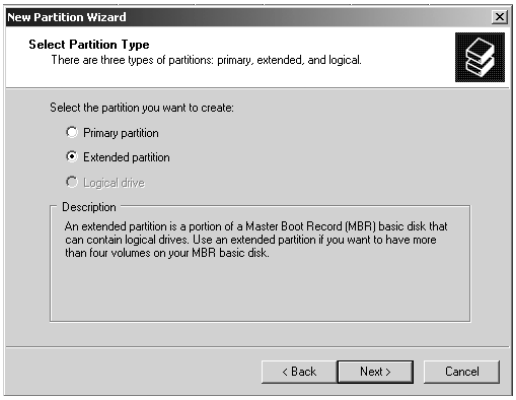
(16) Move cursor to Disk0 unallocated area and press UNDO key, and select “New partition...” on menu.



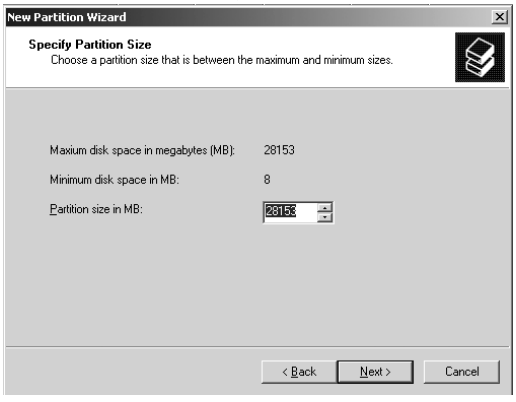
(17) Click “Next>” button.



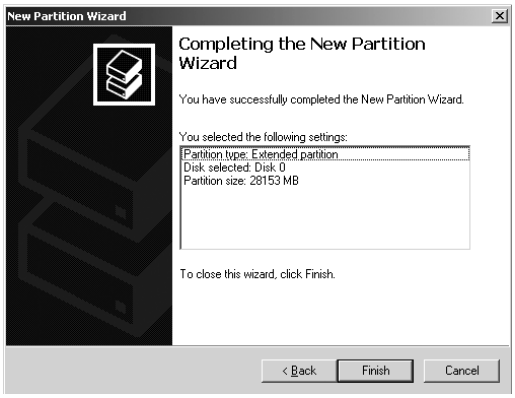
(18) Select “Extended partition” and click “Next>” button.



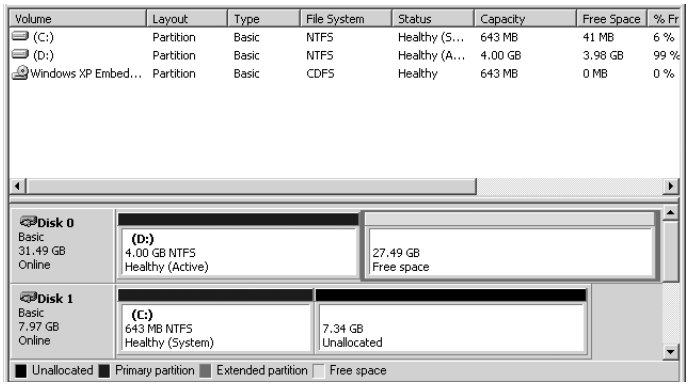
(19) Click “Next>” button. (Partition size is max.)



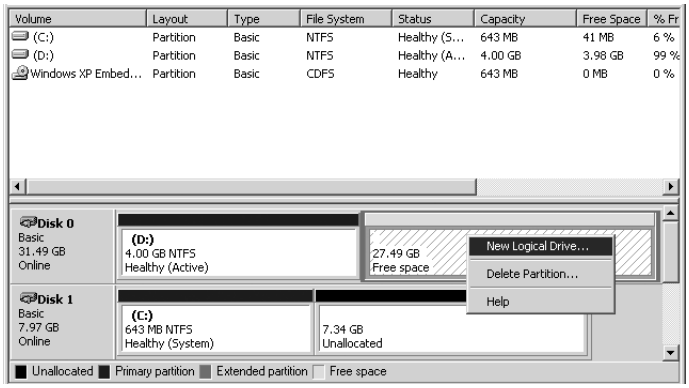
(20) Click “Finish” Button.



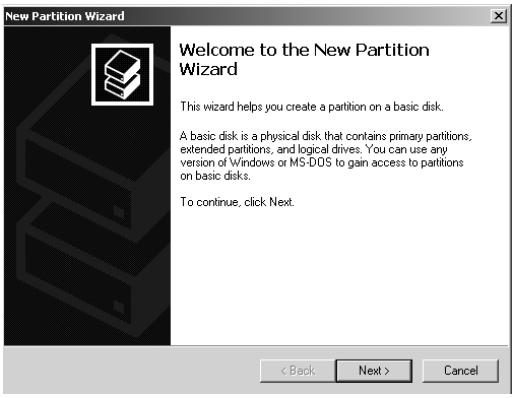
(21) Create the free space in the back of D drive.



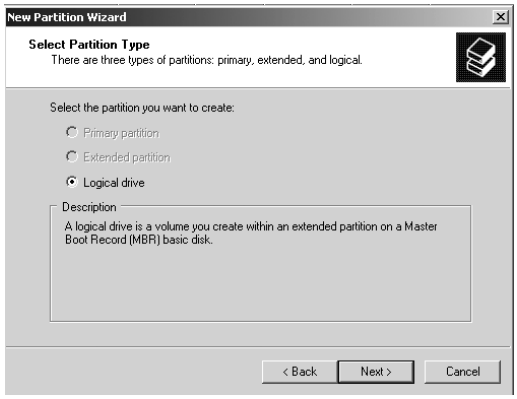
(22) Move cursor to the free space area and press UNDO key, and select “New logical drive” on menu.



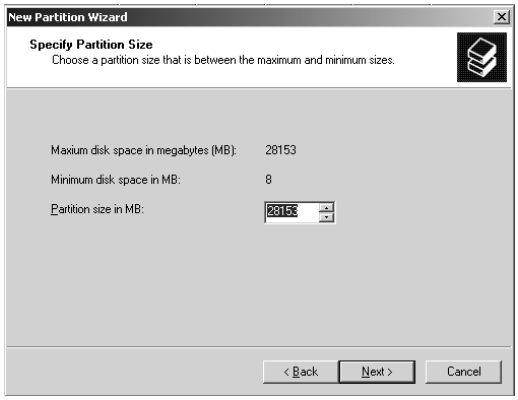
(23) Click “Next>” button.



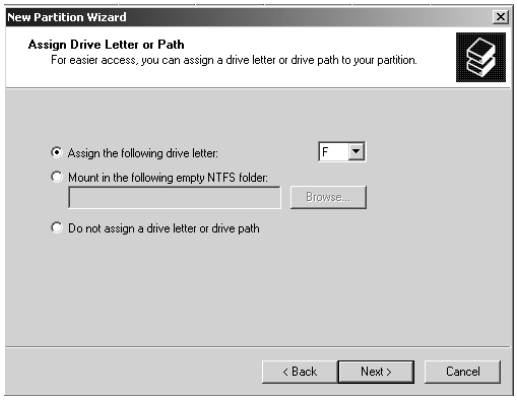
(24) Select Logical drive and click “Next>” button.



(25) Click “Next>” button. (Logical drive size is max.)



(26) Recognized “F” for drive letter and click “Next>” button.

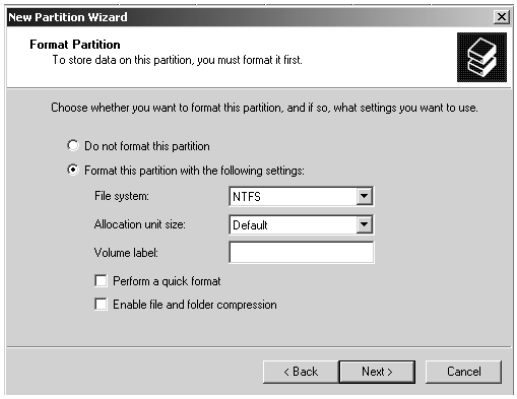


(27) Set item as followings and click “Next>” button.

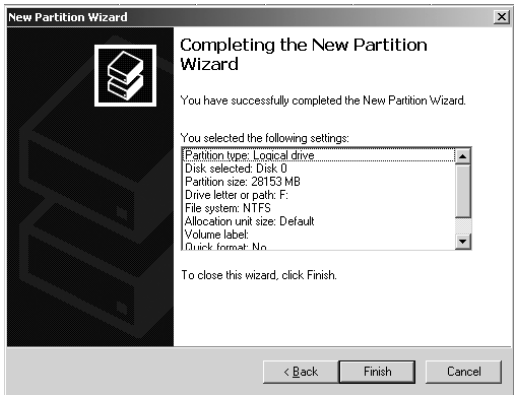
Set File system to NTFS.

Set allocation unit Default.

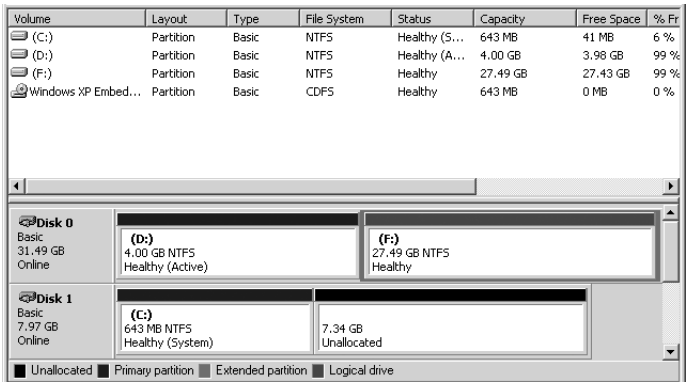
Set volume label to blank.



(28) Click “Finish” Button.



(29) Start F drive formatting and finish to 100% and create area



(30) Turn off diskmgmt.exe dialog, and copy all of Eub-us folder in C:/ to D:/

(31) Double click Eubsys.exe in C:/Install, then install XP Embedded system. Displaying a dialog on installing, but close the dialog when finished.

(32) Depress “Ctrl + Alt + Del” and Displaying Windows security image. And press “Shutdown” button.

(33) Select item of “Shutdown”, Press “OK” button. Then ultrasound equipment is shut downed.

(34) Quite power off and power on ultrasound equipment, and start up it. When displayed bios image of HITACHI logo, immediately take off the System CD by using eject button in front of CD-R/RW drive. After ejected the System CD, closed CD-R/RW tray by using the eject button again.

Note: If success taking off the System CD, start up from installed HDD. If failed taking off the System CD, start up from the System CD. Then turn off the power by using STAND BY SWITCH; repeat same (35) from first.

(35) When displaying the ultrasound start up image, depress “Ctrl + Alt + E”, and then start explorer.exe program. Verified as following item and figure.

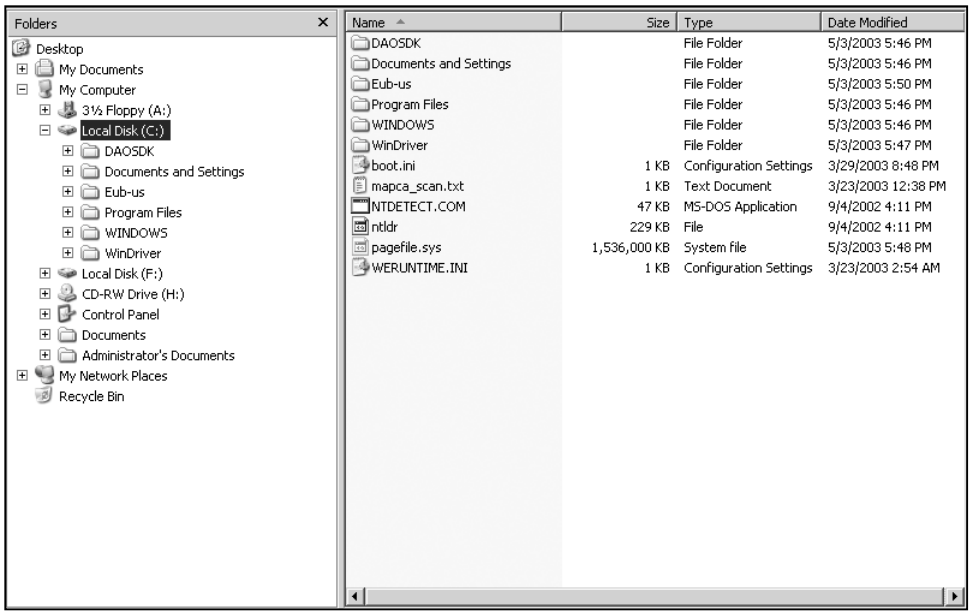
A drive: Floppy Disk drive

C drive: XP Embedded operating system and ultrasound program

D drive: MO Disk drive (Option)

F drive: Ultrasound work area

H drive: CD-R/RW Disk drive



Note1: If the drive letter of device were different, change to correct drive letter by using C:/Eub-us/Tools/diskmgmt (shortcut)

Note2: If displaying dialog of restart up or not, then select “no” for new hardware.

(36) End of install by depressing “Ctrl + Alt + Del”. Refer to item of (33) and (34) in detailed.

3.2.7 Others of "Service Tools"

Functions of (1) ~ (11) of "Service Tools" shown in the figure below:

(1) "Guide line" : Refer to the TECHNICAL GUIDE (Installation).

(2) "Color Bar" : Refer to the TECHNICAL GUIDE (Installation).

(3) "G-Scale" : Refer to the TECHNICAL GUIDE (Installation).

(4) "Diagnostic tests" : Executing the check program(refer to 3.2.5.2)

(5) "Connectable probe list" : Displaying the connectable probe list.

(6) "Event viewer" : Displaying the event log viewer for EUB application software"

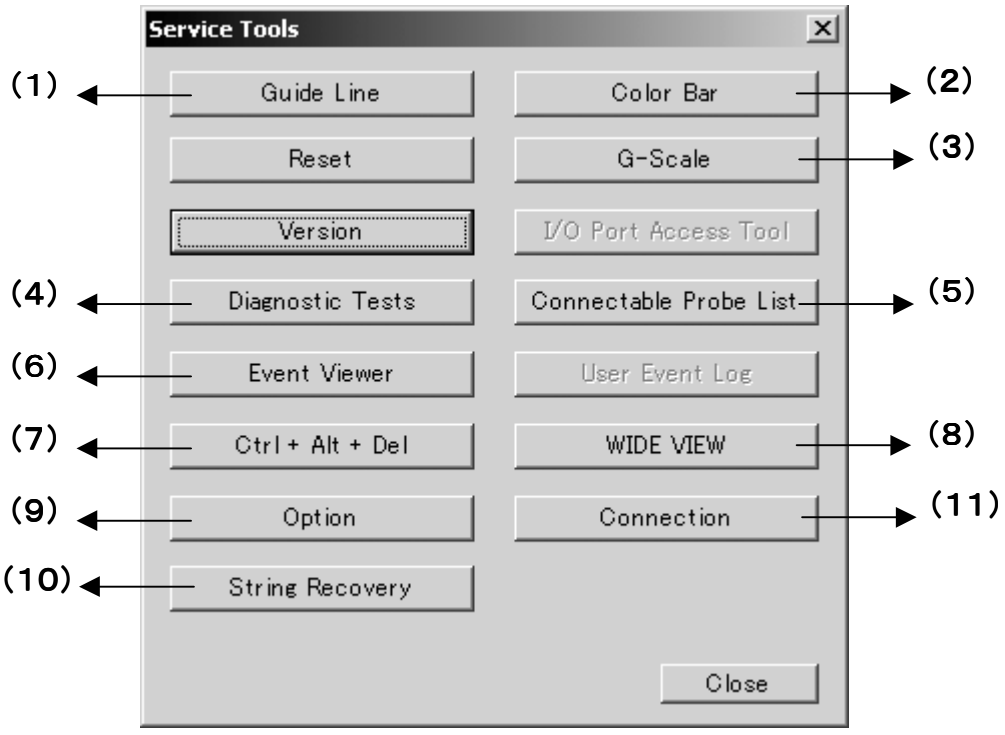
(7) "Cntrl+Alt+Del" : Validating the "Cntrl+Alt+Del".

(8) "WIDE VIEW" :Unusable

(9) "Option" :Unusable

(10) "String Recovery" :Unusable

(11) Connection" :Unusable



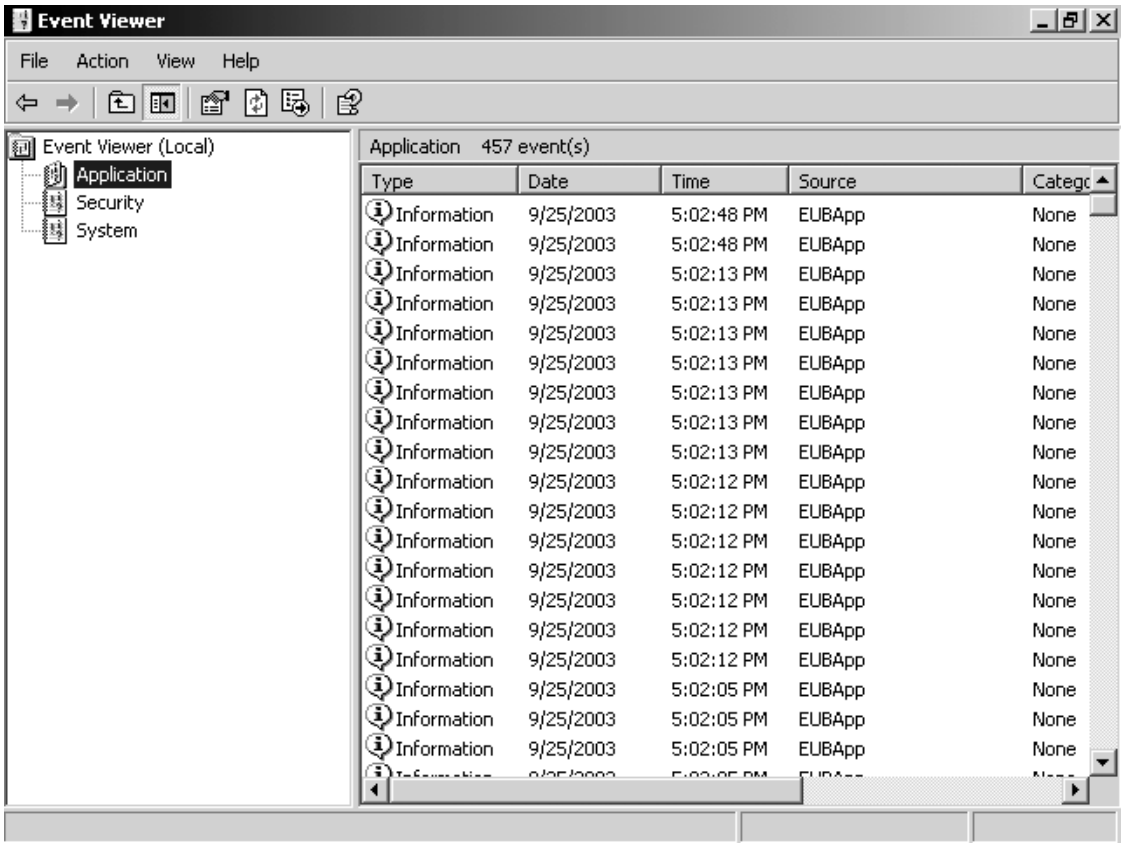
3.2.6 Displaying the error log.

(1) Start the “Service tool” .(Refer to 3.2.1 (1),(2),(3).

(2) Click the Event Viewer button in dialog of service tool.

(3) Select the Application to display the Application log of EUB application software.

(Refer to following)



(4) The following list show the kind of application log.

Event ID	Type	Event log
1	Information	Booting started.
2	Information	Data check started.
5	Information	Booting completed.
6	Information	BackUpDB setup started.
7	Information	ApplicationDB setup started.
8	Information	ApplicationResourceDB setup started.
9	Information	BodyMarkDB setup started.
10	Information	AnnotationDB setup started.
11	Information	FilingDB setup started.
12	Information	MeasureemtnDB setup started.
13	Information	ProbeDB setup started.
14	Information	3DDB setup started.
15	Information	PrinterList setup started.
16	Information	WVDB setup started.
17	Information	PatientMenuDB setup started.
18	Error	Software error occurred.
4097	Information	Backup started.
4098	Information	Backup completed.

4099	Error	Backup error.
12289	Error	No Dus file of the probe selected.
12290	Error	Dus file decompression failed.
12291	Error	Dus file error.
12292	Error	BWDSC file loading error.
12293	Error	CFMDSC file loading error.
12294	Error	DCFM file loading error.
12295	Error	DDOP file loading error.
12296	Error	Smoothing file loading error.
12297	Warning	Probe cannot be selected.
12298	Error	Probe ID error.
16385	Error	PCI-VME error.
16386	Warning	PCI-VME key cannot be opened.
20481	Error	BWDSC PCB is missing.
20482	Error	CONT PCB is missing.
20483	Error	DCSP PCB is missing.
20484	Error	CINE PCB is missing.
20486	Error	CFMDSC PCB is missing.
20488	Error	DVP PCB is missing.
20489	Error	SYSTEM-ID loading error.
20490	Error	VME arbitration error.
20492	Error	Not bus error.
20493	Error	Probe identification failed
20495	Error	MPTEE interface error.
20496	Error	Same value at GND and ST4V.
20497	Error	A/D value at D/A 00 and FF is the same.
20498	Error	CALIB_MINI_0V is smaller than 0.
20499	Error	CALIB_MINI_5V is larger than 255.
20500	Error	ATGC A/D value at D/A 00 and FF is the same.
20501	Error	CALIB_TGC_0V is smaller than 0.
20502	Error	CALIB_TGC_5V is larger than 255.
20503	Error	ATT A/D value at D/A 50 and FF is the same.
20504	Error	CALIB_ATT_0V is smaller than 0.
20505	Error	CALIB_ATT_4V is larger than 255.
20506	Error	LOG data of DVP PCB is wrong.
20507	Error	TGC EXPO data of DVP PCB is wrong.
20508	Error	TGC MANT data of DVP PCB is wrong.
20209	Error	LPF COEF data of DVP PCB is wrong.
20510	Error	DBF1 PCB is missing.
20511	Error	DBF2 PCB is missing.
20512	Error	DBF3 PCB is missing.
20513	Error	DBF4 PCB is missing.
20514	Error	AWP2 PCB is missing.
20515	Error	AWP1 PCB is missing.
20216	Error	CONT PCB configuration error.
20517	Error	DVP PCB configuration error.
20518	Error	DCSP PCB configuration error.
20519	Error	CFMDSC PCB configuration error.
20520	Error	BWDSC PCB configuration error.
20521	Error	CINE PCB configuration error.
20522	Error	AWP1 PCB configuration error.

20523	Error	USSYNC RAM data is wrong.
20524	Error	STCW PCB configuration error.
20673	Error	WinDriver open werror
20674	Error	EPI PCB is not Connected
20675	Error	EPI : Open error.
20676	Error	EPI : Boot error
28677	Error	EPI : DCM error
28678	Error	PRB : Config error.
28679	Error	PRB PCB is not connected.
28680	Error	DBF : Config error.
28681	Error	PRB PCB is not connect.
28682	Error	BIO : Config error.
28683	Error	CW : Config error.
28688	Error	MAP0 : Open error.
28689	Error	MAP1 : Open error.
28690	Error	MAP2 : Open error.
28691	Error	MAP3 : Open error.
28692	Error	MAP0 : Binary file load error.
28693	Error	MAP1 : Binary file load error.
28694	Error	MAP2 : Binary file load error.
28695	Error	MAP3 : Binary file load error.
28696	Error	MAP0 : Boot phase(0) error.
28697	Error	MAP1 : Boot phase(0) error.
28698	Error	MAP2 : Boot phase(0) error.
28699	Error	MAP3 : Boot phase(0) error.
28700	Error	MAP0 : Boot phase(1) error.
28701	Error	MAP1 : Boot phase(1) error.
28702	Error	MAP2 : Boot phase(1) error.
28703	Error	MAP3 : Boot phase(1) error.
28704	Error	MAP0 : SharedParam Write error.
28705	Error	MAP1 : SharedParam Write error.
28706	Error	MAP2 : SharedParam Write error.
28707	Error	MAP3 : SharedParam Write error.
28708	Error	MAP0 : MapStatus Read error.
28709	Error	MAP1 : MapStatus Read error.
28710	Error	MAP2 : MapStatus Read error.
28711	Error	MAP3 : MapStatus Read error.
28712	Error	MAP0 : RunningCount is stopped.
28713	Error	MAP1 : RunningCount is stopped.
28714	Error	MAP2 : RunningCount is stopped.
28715	Error	MAP3 : RunningCount is stopped.
28716	Error	MAP0 : Memory Init error.
28717	Error	MAP1 : Memory Init error.
28718	Error	MAP2 : Memory Init error.
28719	Error	MAP3 : Memory Init error.
28720	Error	MAP0 : Boot error.
28721	Error	MAP1 : Boot error.
28722	Error	MAP2 : Boot error.
28723	Error	MAP3 : Boot error.
28724	Error	Map Chip Count Failed.
28725	Error	Map Liblary read Error.
28726	Error	MAP1 PCB Revision read error.
28727	Error	MAP2 PCB Revision read error.

3. 2. 7. 2 Executing check program,

(1) Start “Service Tools”. --- See 3.2.1 (1), (2) and (3)

(2) Start “Service Tools”. --- See 3.2.1 (1), (2) and (3)

(3) The following functions are available as check programs.

1) RAM Test

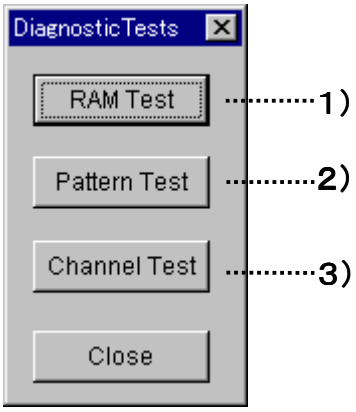
A function to check if the memory that is an important component of each PCB works normally

2) Pattern Test

A function to check if any PCB is faulty by inserting test patterns into plural points in the signal processing line.

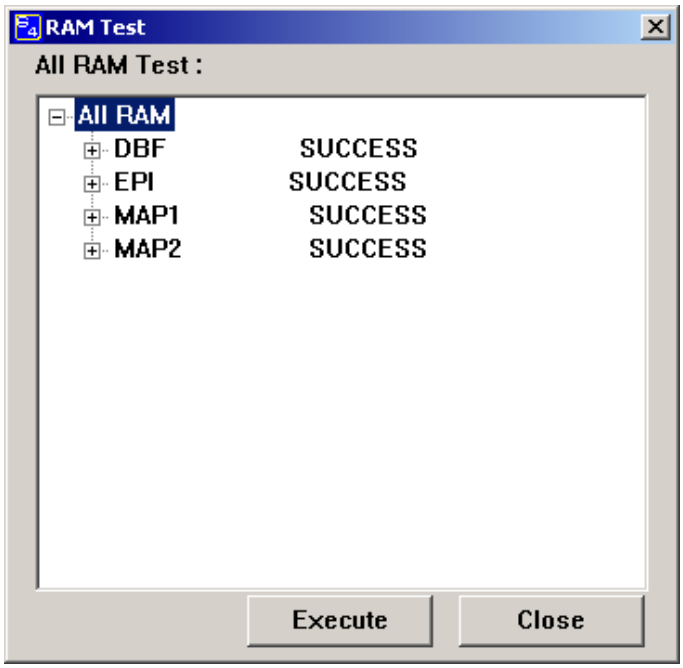
3) Channel Test

A function to check if analog circuits of transmission and reception waves work normally by channel.

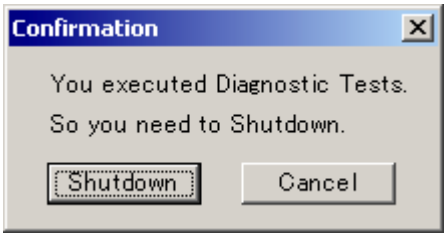


1) RAM Test

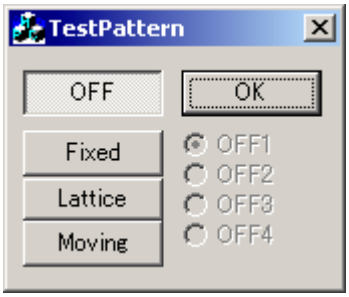
Click the "Execute" button to check the memory. Boards to be checked are DBF, EPI, MAP1 and MAP2 PCB. The result of memory check is displayed as "SUCCESS" or "FAILURE".



After executing memory check, if clicking each button in "Diagnostic Tests" and "Close" button in "Service Tools", the following message is displayed. To return to any normal imaging mode, the system needs to be shut down. Also, after executing memory check, the other check programs (Pattern Test and Channel Test) cannot be used.



2) Pattern Test

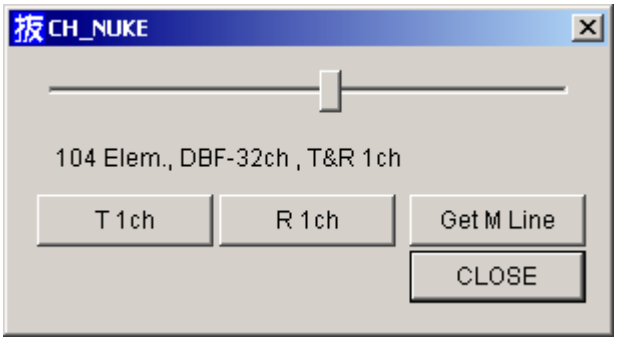


Press each button in the dialog to perform the following operation. Each button has an image mode recommendable; therefore, the Test Pattern dialog needs to be displayed after selecting t

he image mode in advance.

button	action	recommended mode
Fixed	Displaying gradation pattern	B mode
Lattice	Displaying the lattice pattern.	B mode
Moving	Displaying the moving an axial beam on US image. Or the test pattern for a scan is displayed every [which was defined] number of scan.	B mode
OFF	All test pattern is terminated and return normal condition.	
OK	Test pattern is erased and return to dialog.	

3) Channel Test



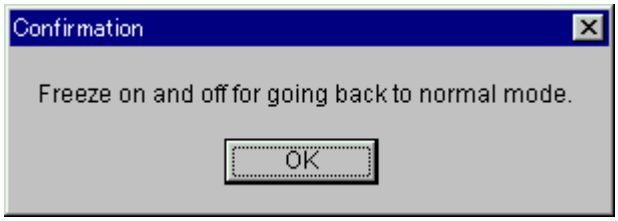
The dialog above allows you to depict a B-image with the transmission wave at the center 1ch and aperture 1ch. Since aperture of the transmission wave is 1ch, if the transmission wave circuit is missing by even 1ch, it can be observed as a dark line in the B-image. Further in the M-image, an image can be depicted using a specific 1ch, so any missing channel may be identified. As well as for the reception wave, any missing channel can be checked.

To implement this test:

① Connect any probe with no missing channel and select the B/M real mode.

② Click “Channel Test” from “diagnostic Tests”. Display Channel Test and set the transmission wave or reception wave to 1ch, and check any missing channel by operating the slide bar at the top of dialog. At this time, if the M-image shows any dark line, it means a missing channel. Note that, however, an element of the probe itself can be faulted.

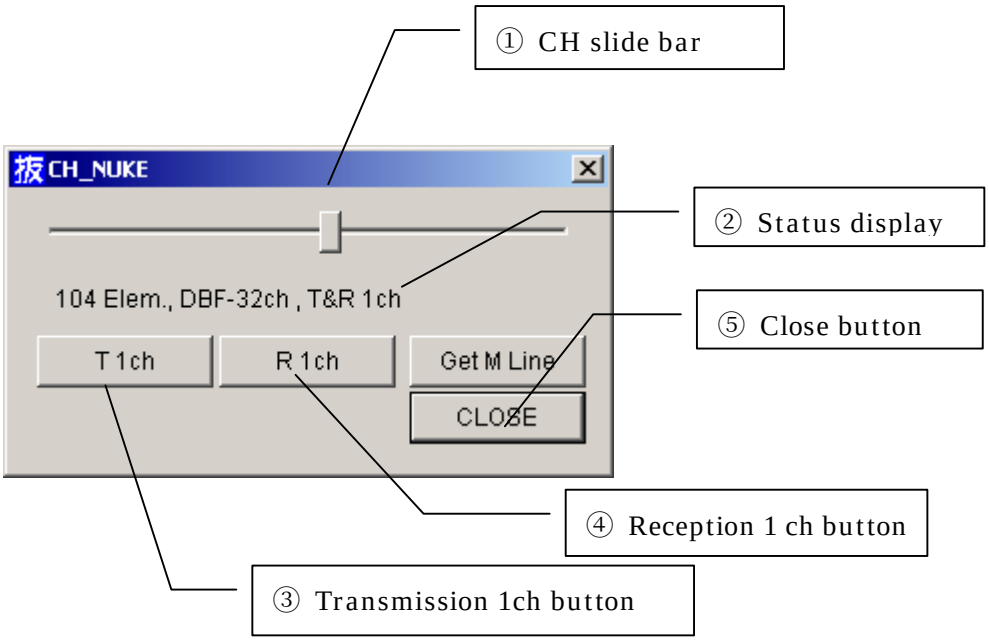
③ After completing the check, close the dialog and click the “Close” button in “Service Tools” to display the following message. To return to the normal imaging mode, the system needs to be freeze ON/OFF.



NOTICE: After completing the check, close the dialog and click the “Close” button in “Service Tools” to display the following message. To return to the normal imaging mode, the system needs to be freeze ON/OFF.

Above action is needed every transmission or reception check.

The following details display and operations:

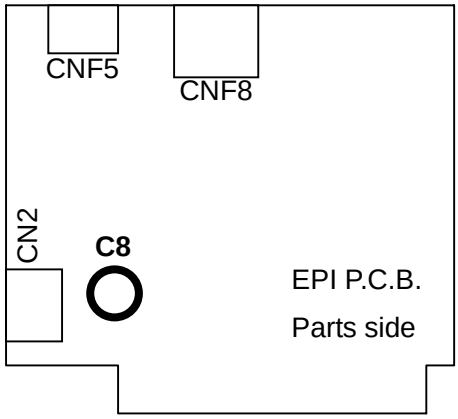


Item	Explanation
① CH slide bar	Selects No. of any element to be checked. No. of the element thus selected is displayed as the Elem. item of ② Status display. This number is from 0 to 191.
② Status display	**1st item (Elem.):** Represents No. of the element for check selected with the CH slide bar. **2nd item (ch):** Represents corresponding to element CH No. in DBF. CH No. is from 0 to 47. **3rd item:** None/No check mode, T 1ch/Transmission wave check mode, R 1ch/Reception wave check mode, T&R 1ch/Transmission and reception wave check mode
③ Transmission 1ch button	Sets the transmission wave to 1ch. The last item of Status display changes to "T 1ch" or "T&R 1ch". Pressing this button allows any missing channel of transmission or reception wave to be checked.
④ Reception 1ch button	Sets the reception wave to 1ch. The last item of Status display changes to "R 1ch" or "T&R 1ch". Pressing this button allows any missing channel of reception wave to be checked.
⑤ Close button	Closes this dialog.

3.2.8 Cautions in replacing EPI PCB

(1) When replacing the EPI PCB, be sure to turn off the breaker switch located at left side of the system.

(2) EUB-5500 is numbered as individual ID number for each system, and this ID number is recorded in ID chip which is equipped on the EPI PCB. (Location on the PCB C8 : Refer to the figure below.)
In case no ID chip is equipped or an incorrect ID chip for different system is equipped, the system does not operate correctly. When replacing EPI PCB, make sure to re-equip this ID chip onto the new PCB to be replaced.



3.2.9 Backup battery

EUB-5500 is provided with the backup battery inside the equipment, which backs up data such as date and time and so on.

The life of this battery is about three years, but it may differ according to usage of the equipment.

When this backup battery reaches its life, booting stops at the screen shown in Fig. 3.2.9-1 when powered on. Follow the steps below to replace the backup battery.

A message “CMOS checksum bad – Default configuration used

Fig.3.2.9-1

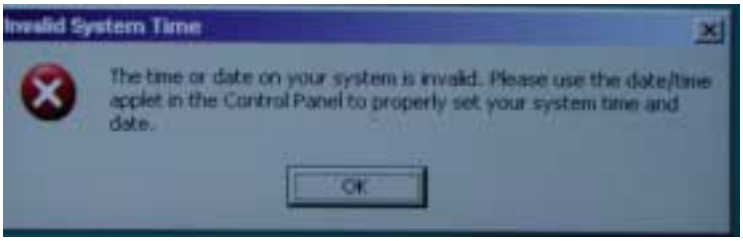
(1) Turn the breaker switch OFF at the left side of the equipment.

(2) Refer to [3.2.10 Replacing the backup battery] for replacing it with a new one.

(3) If booting the equipment after replacing the backup battery, booting stops at the screen shown in Fig. 3.2.9-1 .

Press “Ctrl + Alt + Shift” key and then “1” key to continue booting.

(4) In the midway of booting, the following dialog appears. Press the “OK” button.



(5) After booting the equipment, refer to (Subsection 7.10 of [Section 7 Main Menu]) for setting date and time.

(6) See the instruction manual to check if the equipment works normally.

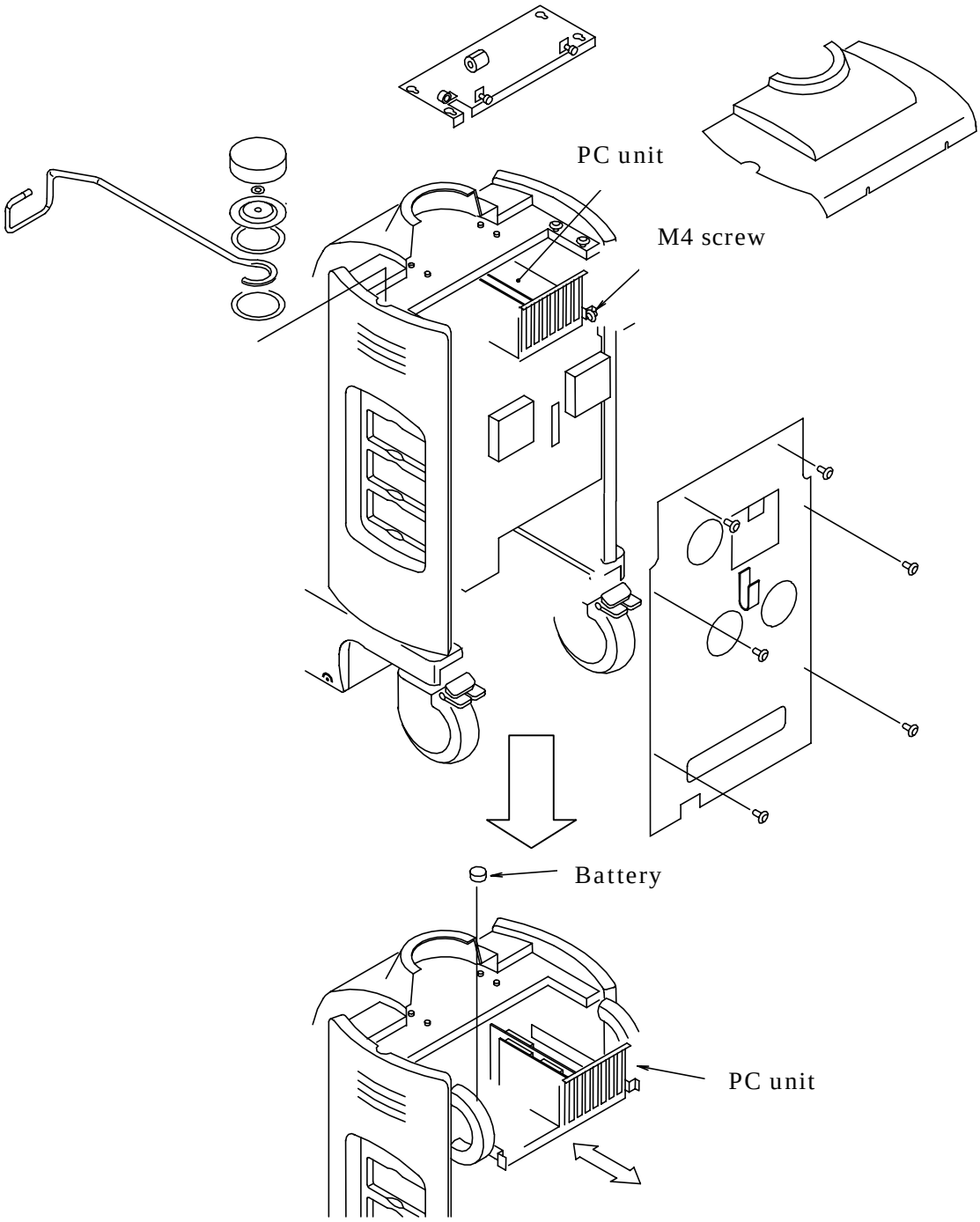
This completes replacing the backup battery.

3.2.10 Replacing the backup battery

(1) Remove the covers.

(2) Disconnect cables, loose M4 screws and withdraw the PC unit.

(3) Replace the battery and restore the cables and covers to their original positions.
(The battery may be replaced without removing the monitor.)



Section 4 Principle of Operation

4.1 System Block of EUB-5500

Fig. 4.1.1 shows the system block diagram of EUB-5500.

★ EUB-5500 uses many hardware parts configurable (programmable) by the configuration data (program data) such as FPGA and DSP on each PCB.

★ mounted on PCB, and FPGA or DSP is configured (programmed) during reset period after booting the system.

4.2 Basic Composition of EUB-5500

4.2.1 General and board description

Composition: PCBs and units composing the basic part of EUB-5500 are listed below:

1. PC unit
2. KB & KBIF
3. PRBSW unit
4. DBF
5. EPI
6. MAP
7. CNPNL

Overview of units and PCBs:

1. PC unit

With WindowsXP as OS, the PC unit runs a variety of application software to control the ultrasound scanner as well as interfaces with various media.

A standard PC structure is added with the following two PCI bus add-in boards in EUB-5500.

Video board : Displays ultrasound image data entered from MAP PCB overlaid on the computer screen. Also, outputs and inputs TV signals for VCR playback and recording.

SCSI Card (Option : EZU-PI1)
: Used to connect with SCSI accessory units. This is necessary for the connection with SCSI printer.

2. KB & KBIF

   Interfaces each key and switch on the control panel with the PC unit.

   Also controls turning on LED.

3. PRBSW

   A section to interface with the probe, which corresponds to the transmitter/receiver of ultrasound scanner.

   PRBSW gives high voltage pulse to the transducer for driving it, as well as amplifies echo returned from body tissue.

   Also, PRBSW is composed of the following two boards:

   (1) PRB PCB
   (2) AWP PCB

4. DBF

   Outputs transmit signals delayed for each channel to PRBSW PCB, beam-formes the received wave signals and sums for channels, and outputs it to EPI PCB.

5. EPI

   Processes each beam-formed signal of B, M, D and CFM mode from DBF, and outputs to MAP.

   And controls ultrasound transmit/receive focusing and generates various control signals for ultrasound scan.

6. MAP

   After applying smoothing, enhancement and so on to image data from EPI PCB, it converts them to TV synchronized signals to output them to the Video Board together with ECG and heart sounds waveform data from BIO PCB.

7. CNPNL

   Connects with external peripheral equipment.

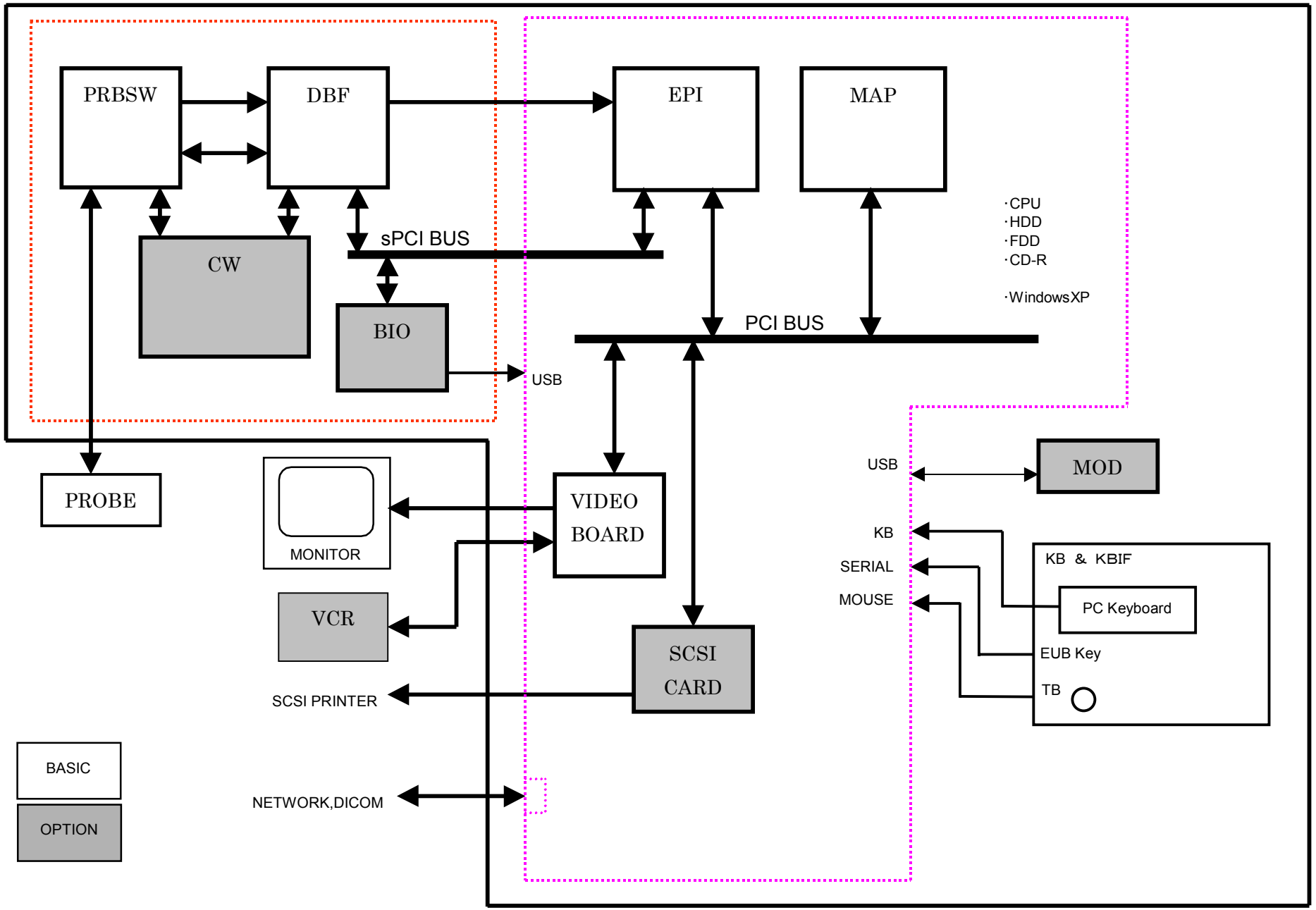


Fig. 4.1.1 EUB-5500 BLOCK DIAGRAM

4.2.2 PRBSW unit circuit description

PRBSW unit is divided into the following 7 blocks.

1. PROBE CONNECT (Probe connector block) (*PRB PCB*)

   Interfaces with the probe.

   EUB-5500 can connect three probes.

2. SEL_SW & RELAY (High voltage SW and relay block to switch the vibrator) (*PRB PCB*)

   A circuit to connect 48CH of transducer elements for transmit/receive out of maximum 192CH of transducer elements with the transmit/receive circuit system.

   One system is provided for PROBE1 and 2, and one for PROBE3. Connection with PROBE1 and PROBE2 is switched by a relay.

3. T_AMP (Transmit AMP block) (*AWP PCB*)

   A circuit to amplify transmit signals sent from DBF PCB.

   Amplified signals drive the transducer as transmit signal.

4. T/R_DIV (Transmit/Receive separating circuit block) (*AWP PCB*)

   A circuit to separate extremely fine receive signal from high voltage transmit signal. Also, it is mounted with an attenuation circuit to prevent waveform of receive signals adjacent to those of high level from distorted due to amplification by PreAMP and gain control AMP.

5. PREAMP (Primary stage amplifier block) (*AWP PCB*)

   A circuit to amplify receive signals by 26dB.

6. TGCAMP (Gain control amplifier block) (*AWP PCB*)

   An amplifier to amplify receive signals according to setting of B-Gain in order to create optimum image by setting receive signal to appropriate input voltage level for the AD converter.

   It realizes uniform images by varying amplification factor in the depth direction.

7. R_FIL (Reception wave filter block) (*AWP PCB*)

   A filter circuit to remove a phenomenon called aliasing that occurs when the AD converter (Analog to Digital) converts receive signal.

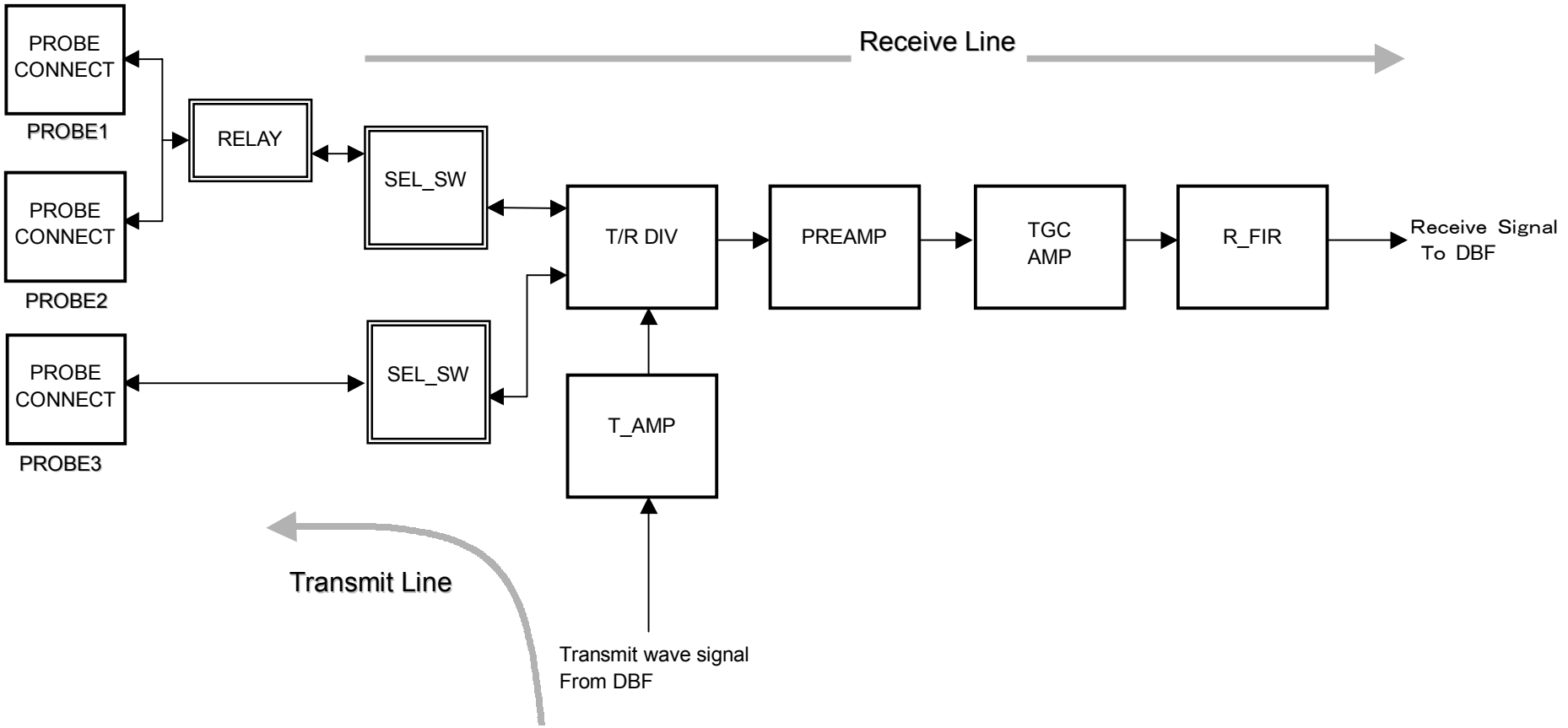


Fig. 4.2.1 PRBSW unit Block Diagram

4.2.3 DBF PCB circuit description

DBF PCB is divided into the following 4 blocks.

1. Digital Beam Former ASIC (Transmit/Receive beam forming block ・・・ ASIC)

   Generates transmit wave signals based on ultrasound transmit focus data.

   Also, beam-formes received signals based on receive focus data then demodulates them and outputs to EPI PCB as complex signal of I and Q.

   Transmit and receive wave focus data is stored in SRAM.

2. AMP (Transmit signal output block)

   Amplifies an analog signal (transmit signal) outputted from ASIC by about twofold and outputs to AWP PCB.

3. ADC (A/D converter block)

   Converts received signal (analog signal) outputted from PRBSW PCB to digital signal and outputs to ASIC.

4. ASIC Controller (Control block)

   Controls interface to sPCI BUS (cf. Section 4.2.4) and each ASIC and SRAM.

5. DUS Controller(Digital US control block)

   Following instructions on the type of ultrasound beam and shot direction outputted from US-Scan Controller of EPI PCB, it controls PRBSW PCB and DBF PCB. Digital control to PRBSW PCB is through serial communication.

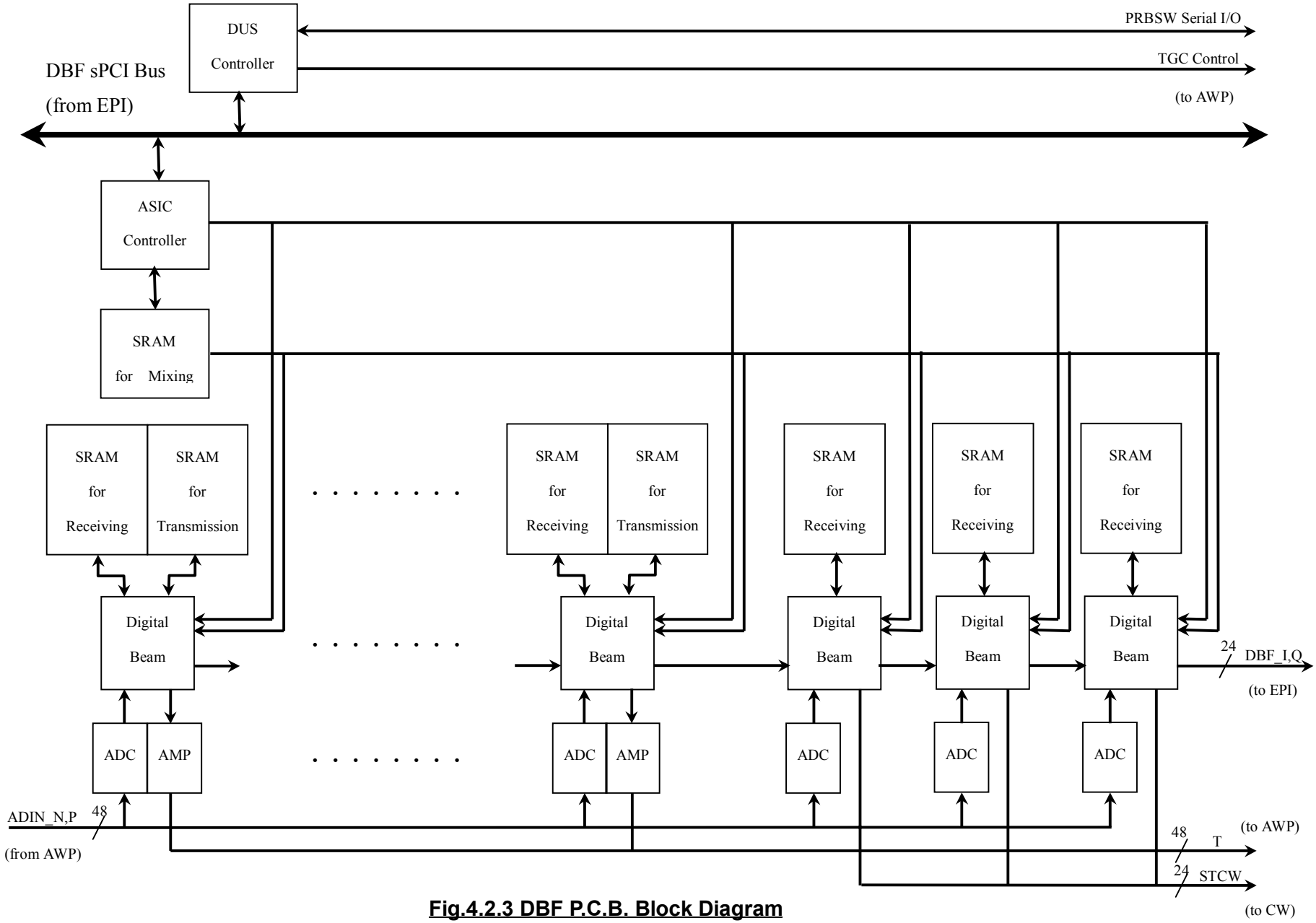


Fig.4.2.3 DBF P.C.B. Block Diagram

4.2.4 EPI board circuit explanation

EPI Board consists of next 14 blocks.

1. P/S Conv.(Parallel Serial Conversion)
   The Parallel complex data from DBF Board is converted to Serial complex data in this block.

2. LPF（Low Pass Filter）
   Filter processing of the complex data from PS Conv Block is carried out by this LPF.

3. Decim（Decimation:Data Pick Up）
   The number of Filtered data is lessened according to display depth. The number changes also with the sizes of CFM ROI..

4. WPI（RF Interpolation & Pulse Inversion）
   Processing of RF Interpolation or Pulse Inversion is performed.

5. Digital-TGC（Digital Time Gain Control）
   Digital Time Gain Control is performed at the time of a B(M)-mode.

6. TCI I/F（TCI Bus Interface）
   The data after signal processing is changed into a TCI Bus format, and it transmits to a MAP Board.

7. US-Scan Controller (US scanning controller)
   The kind of ultrasound beam, the transmitting direction, and data taking-in timing of signal processing blocks is controlled by DMA sequencer.

8. US-SYNC Generator (US synchronized signal generator)
   It generates the signal which synchronized with ultrasonic transmission of Y-SYNC* etc. according to PRF.

9. CLK Generator (Generating Clocks)
   From a 125MHz crystal oscillator, it generates 8ns, 16ns, 20ns, 32ns, 40ns, 64ns, and the 4 time cycle clock of transmitting frequency. Clock to other boards is outputted by LVDS.

10. PCI Bridge

It connects EPI Board to the PCI bus of the system PC section.

11. sPCI Bridge

It connects EPI Board to the DBF and BIO Board by sPCI Bus. Therefore, port I/O of their Board can be accessed from PC.

12. Audio DAC (Audio Signal D/A Converter)

D/A conversion of the Digital Doppler Audio signal (IIS Format) is carried out for a speaker output.

13. SIG SEL & AMP（Select Signal of speaker output & Audio amplifier）

The L/R stereo signal inside a EPI Board and the L/R stereo signal from the outside are changed, and electric power amplification for driving a speaker is performed.

14. System ID

The equipment ID which can be read from software is given using ID chip.

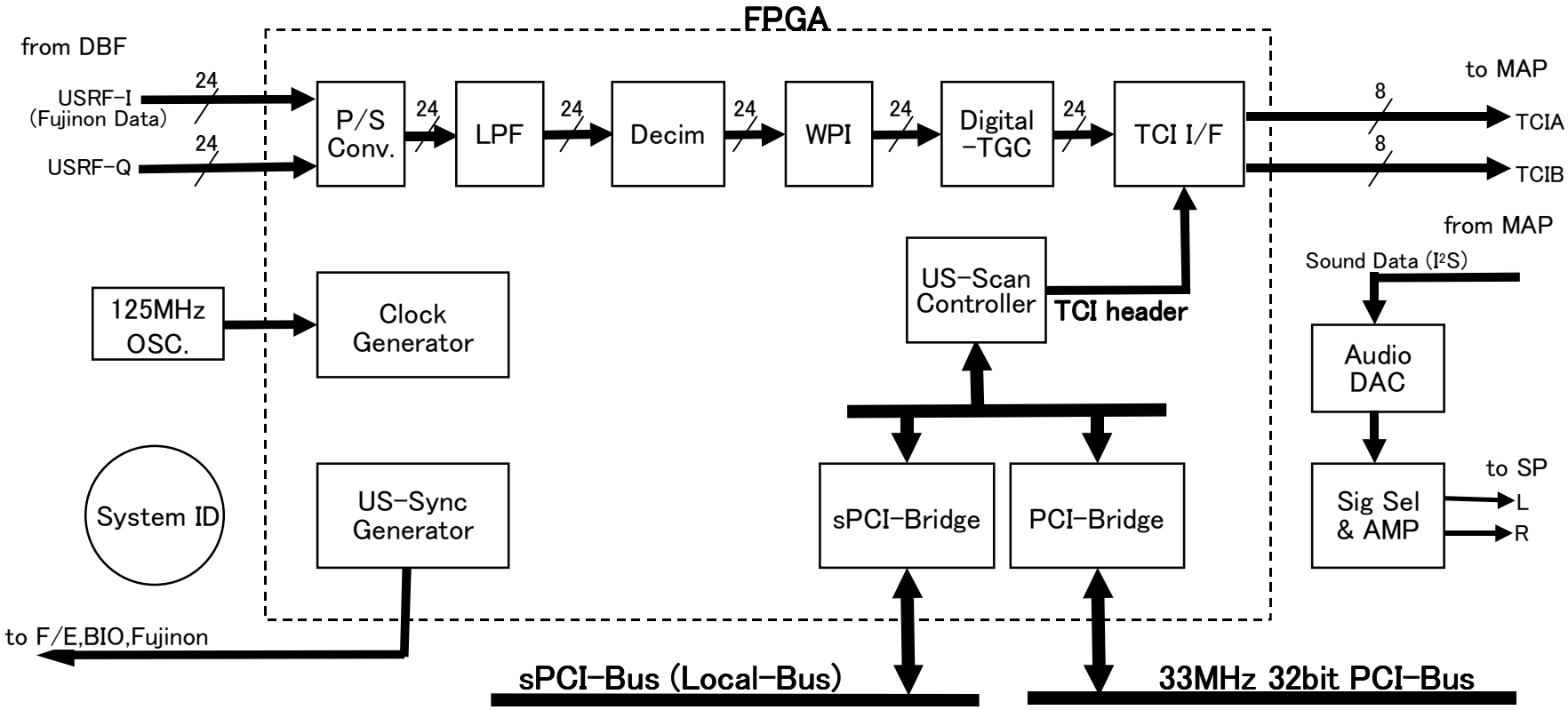


Fig4.2.3 EPI PCB Block Diagram

. 4.2.5 MAP PCB circuit description

4.2.5.1 General Description

MAP PCB is divided into the following 6 blocks.

These 6 Blocks are processed by four MAPs (Media Accelerated Processor) carried in two MAP PCBs.

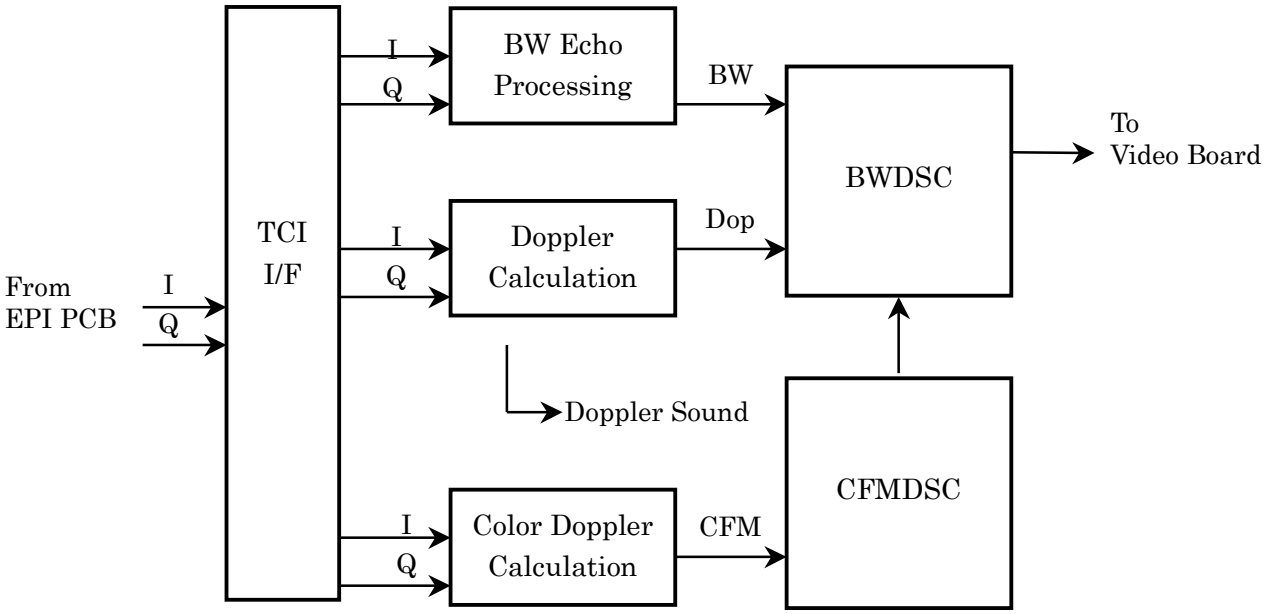


Fig4.2.4 MAP PCB Block Diagram

1. TCI I/F

   This block extracts monochrome data, Doppler data and CFM data from the TCI (Transport Channel Interfaces) data from EPI PCB.

2. BW Echo Processing

   This block calculates monochrome scalar data from complex data.

3. Doppler Calculation

   This block calculates pulse wave Doppler data or continuous wave Doppler data from complex data.

4. Color Doppler Calculation

   This block calculates CFM data from complex data.

5. CFMDSC

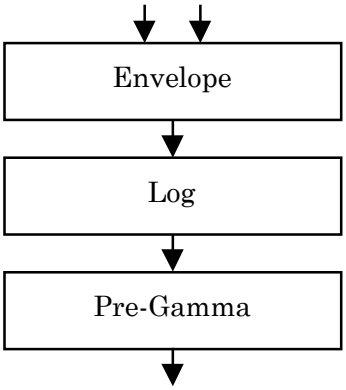
   This block performs image processing such as smoothing and SCC to CFM data, and constructs a CFM image data by Scan Conversion.

6. BWDSC

   This block performs image processing, such as Enhance and SCC to monochrome data, and constructs a monochrome image data by Scan Conversion. And monochrome image data is compounded with the CFM image data from the CFMDSC block, and is transmitted to a video board.

4.2.5.2 BW Echo Processing

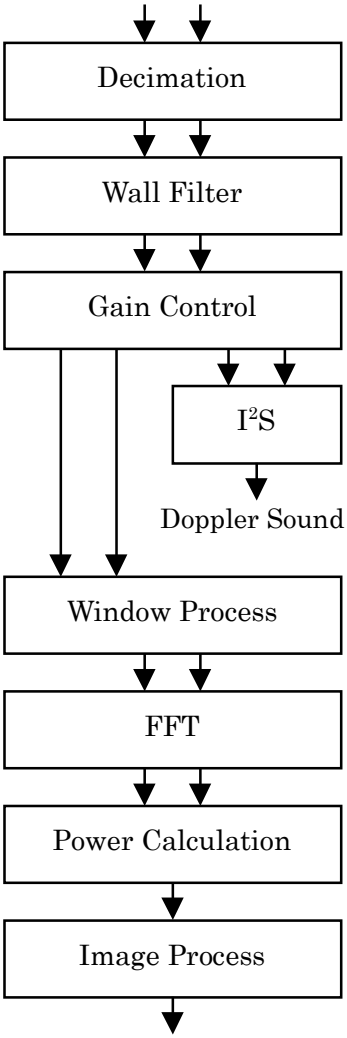
A processing flow is shown in the following



1. Detects envelope by orthogonal detection for complex data.
2. Applies logarithmic compression to image data that is now intensity information.
3. Applies gamma correction to image data applied with logarithmic compression.

4.2.5.3 Doppler Calculation

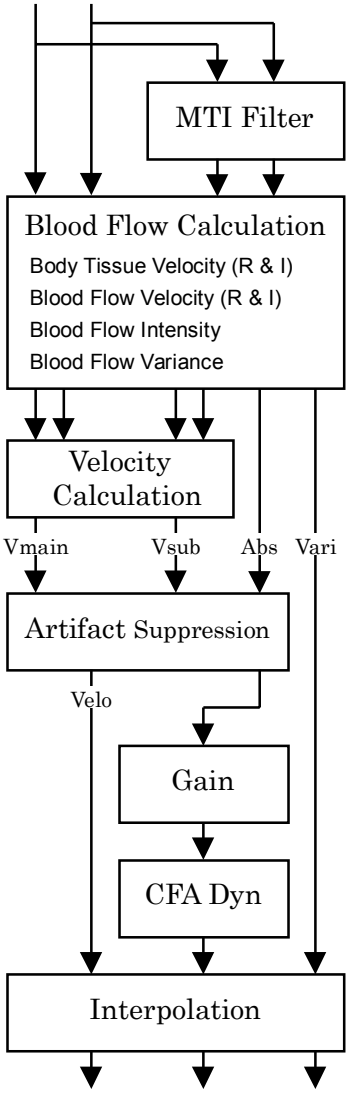
A processing flow is shown in the following



1. Decimates complex data
2. Removes low frequency signal components from Doppler data by high pass filter.
3. Amplifies and attenuates Doppler data.
4. Converts Doppler sound data into I^2S(Inter IC Sound) data.
5. Multiplies Doppler data by window function.
6. Carries out frequency analysis of Doppler data based on the Fast Fourier Transformation (FFT) algorithm.
7. Calculates brightness of each frequency component from Doppler complex signal.
8. Applies image processing such as MAX sampling and gamma correction to Doppler data.

4.2.5.4 Color Doppler Calculation

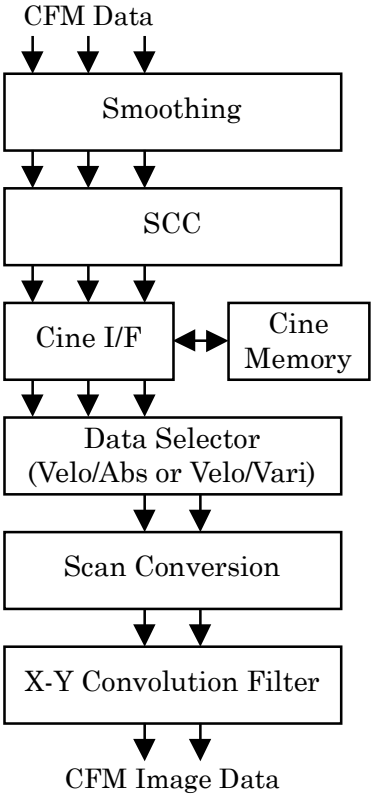
A processing flow is shown in the following



1. Removes unnecessary low velocity signal components form body tissue structure such as cardiac wall.
2. Calculates complex signal of velocity of body tissue motion from through the MTI filter, and calculates complex signal of velocity of blood flow, instantaneous reflection intensity of blood flow and velocity variance of blood flow from MTI filter.
3. Calculates average velocity of body tissue motion and average velocity of blood flow.
4. Suppresses CFM artifacts from average velocity of body tissue motion, average velocity of blood flow and reflection intensity of blood flow.
5. Amplifies and attenuates CFM data.
6. Calculates CFA dynamic range in the CFA mode.
7. Interpolates complex data of body tissue velocity, complex data of blood velocity, reflection intensity of blood flow and velocity variance of blood flow in the beam direction to double the number of lines.

4.2.5.6 CFMDSC

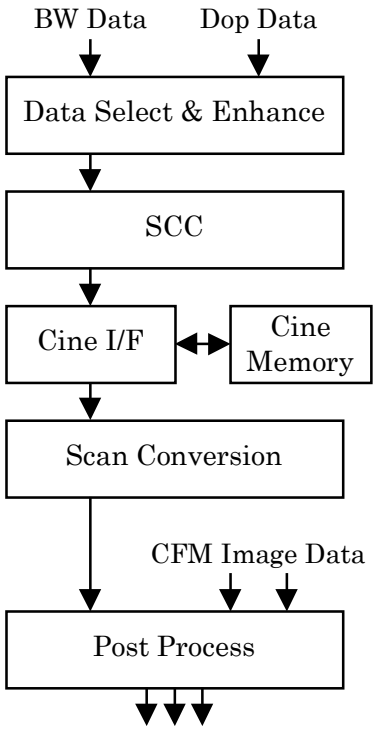
A processing flow is shown in the following



1. Applies smoothing process by median filter or Convolution filter
2. Applies frame correlation process.
3. Interfaces with Cine Memory.
4. Selects two data from velocity data, velocity variance data and reflection intensity data according to color map.
5. Constructs a CFM image data by Scan Conversion and Affine transformation.
6. Applies smoothing process to a CFM image data.

4.2.5.7 BWDSC

A processing flow is shown in the following



1. Selects monochrome data or Doppler data and applies enhance process.
2. Applies frame correlation process.
3. Interfaces with Cine Memory.
4. Constructs a monochrome image data by Scan Conversion and Affine transformation.
5. Applies post process and RGB conversion to monochrome image data and color image data, compound image, and transfer to a video board.

4.2.6 KB & KBIF PCB description

4.2.6.1 KB

Provides appropriate keystroke, key click and illumination by backlight LED as an control panel of rubber sheet.

(1) LED
Two types of red and green LED. Turned ON/OFF according to the key status.

(2) Key switch
Depressing the key switch outputs ON and releasing it outputs OFF signal.

(3) Toggle switch
Pressing upward or downward the toggle switch outputs ON signal and returning to the center outputs OFF signal.

(4) Rotary encoder
Depressing the rotary encoder outputs ON signal and releasing it outputs OFF signal.

Turning the rotary encoder clockwise outputs positive value and counterclockwise negative value.

(5) Slide variable resistor
Variation of resistance outputs variation of data value.

4.2.6.2 KBIF PCB

Controls overall keyboard unit for communication with the main unit (RS232C, PC/2 keyboard, PS/2 mouse) and processes corresponding to each command.

(1) Key scan
Depressing the key obtains a key scan data from the scan line output.

(2) Rotary switch and rotary encoder scan
Depressing the rotary switch detects signals and recognizes the rotary switch selected to make it ON. Releasing it makes it OFF.

Setting data to any specific address selects a rotary encoder to obtain data from the specific address.

(3) Slide variable resistor scan
Periodically obtains data of the slide variable resistor converted by the A/D converter built in CPU.

(4) Interruption process by each signal
Depressing the FREEZE key obtains data from IRQ6.

SYNC_ERR signal acquires data from IRQ5 based on data sent from the system.

R-wave trigger signal acquires data from IRQ7 based on data sent from the ECG unit.

SPARE0 and 1 signals acquire data from the data bus based on data sent from the system.

(5) PS/2 keyboard interface
Acquires a control command for the OADG standard section of the keyboard by communicating with the system via the PS/2 keyboard interface.

Transmits data detected by key scan (OADG standard keys) to the system.

(6) RS232C serial interface
Communicates with the system via the RS232C serial interface to acquire a control command for the supplementary function section.

Transmits data detected by key scan (exclusive keys for EUB), rotary switch scan, rotary encoder scan, slide variable resistor scan, etc.

(7) Version signal readout
Acquires data from a specific address when turning ON the power.

(8) ON/OFF control of key switch LED
Controls backlight LED (green and red) of keys on request from the system.

(9) Buzzer output control
Sounds the buzzer when detecting key ON.

4.2.6.3 TR unit

Turning the ball acquires relative coordinates in the X and Y directions and outputs data. In addition, takes in signals corresponding to 2 buttons and outputs them.

(1) Receiving data
Communicates in the serial interface of clock sync to set transmission parameters based on commands from the main unit.

(2) Transmitting data
Communicates in the serial interface of clock sync to transmit button, XY sign and XY overflow data in the 1st byte, and relative coordinate data in the X direction in the 2nd byte and relative coordinate data in the Y direction in the 3rd byte.

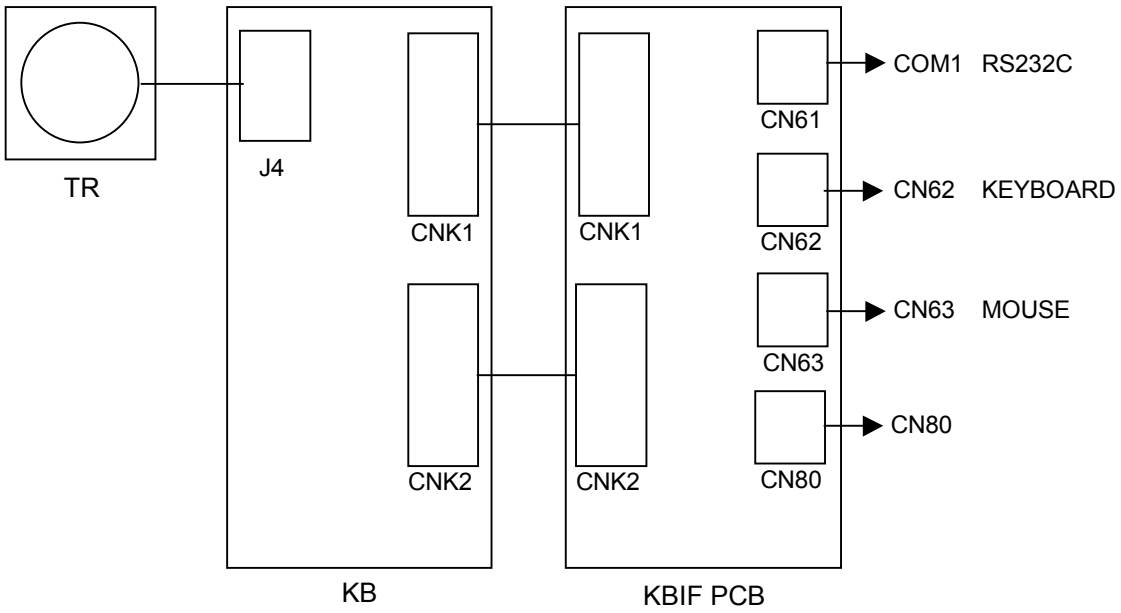


Fig. 4.2.5 Keyboard Unit Block Diagram

4.3 BIO Unit EZU-EK25

4.3.1 General and board description

Composition : EZU-EK25 is an option of EUB-5500 and consists of the following PCB.

1. BIO PCB

Outline of PCB : The PCB executes amplification and filter process of ECG signal, and controls for display on the monitor.

4.3.2 BIO PCB circuit description

BIO PCB is divided into the following 14 blocks.

1. Instrumentation Amp.

   Amplifies the signals obtained from 3 ECG electrodes.

2. Amplifier

   Amplifies ECG signal.

3. Volume control

   Adjusts the ECG signal to an appropriate volume.

4. Filter

   Cuts high frequency with the filter.

5. R-WAVE

   The comparator to pick up R-wave from ECG signal.

6. A/D converter

   A/D converts the signal outputted from the analog part.

7. Digital filter

   Digital processing of a low path filter, a high path filter, a position variable, a notch filter, etc. is carried out to the A/D converted data.

8. R-Trig control

   Outputs R-Trig signal corresponding to ECG ON/OFF.

9. Clock generation circuit

   Produces the reference clock (10msec) for Sync1, Sync2 and Heart rate measurement.

10. Delay counter

    Counts down the value given from the CPU and produces Sync1 and Sync2 signals.

11. Sync 1 / 2 circuit

    Makes the control signal when scanning the US signal with Sync mode and also produces the control data for display of Sync mark on BIO waveform displayed on the monitor.

12. Heart rate counter

    Counts the time between R-wave and next R-wave of ECG waveform and read its counted value with CPU to measure the heart rate value.

13. Time-stamp controller

    Controls the signal showing the time which synchronized with US Image,

    and makes Time-stamp data in accordance with the timing of ECG data creation.

14. USB data generator

    Makes the serial data for USB transmission of the Time-stamp data, ECG data,

    SYNC 1/2 and R-trig signal.

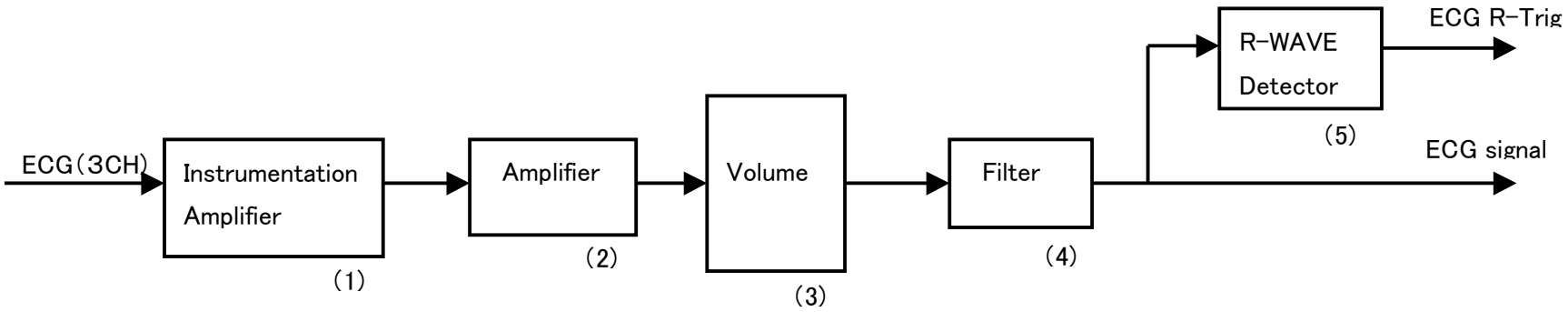


図4.3.1　BIO P.C.B. Block Diagram 1

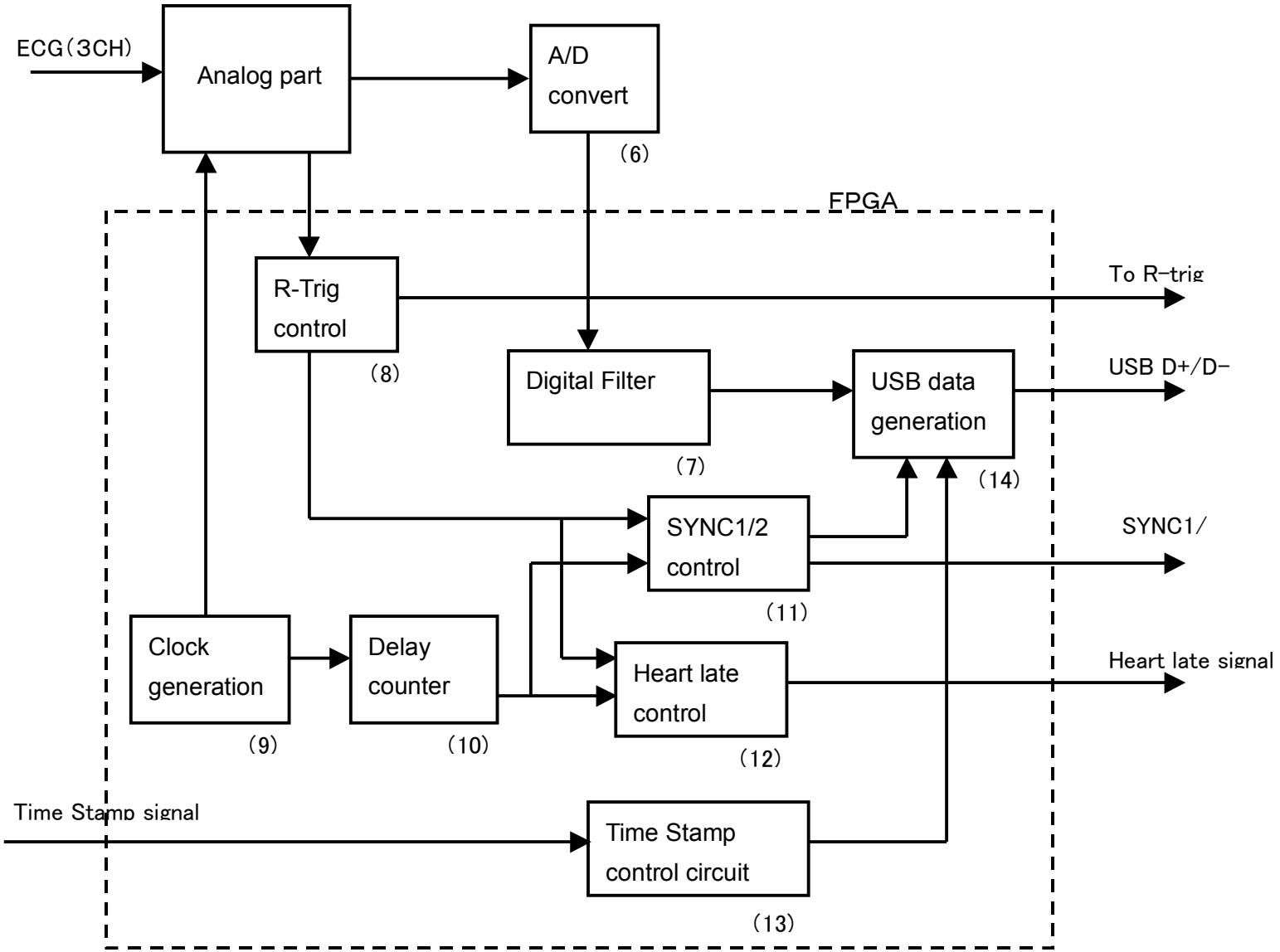


図4.3.2 BIO P.C.B. Block Diagram 2

4.4 Steerable CW Doppler Unit EZU-ST5

4.4.1 General and board description

Composition : EZU-ST5 is an option of EUB-5500 and consists of the following PCBs.

1. CW PCB

Outline of PCB : This is for steerable CW Doppler by sector probe. CW PCB carry out phase arrangement, addition, demodulation and filter process.

4.4.2 CW circuit description

CW PCB is divided into the following 11 blocks.

1. TRANSMITTING BUFFER (Transmitting buffer part)

   A buffer to drive transmit Amp of AWP P.C.B., to the transmit signal sent from DBF P.C.B.

2. MIXER (Demodulation circuit part)

   Detects the element of Doppler shift by mixing with the reference wave.

3. HIGH PASS FILTER (High frequency pass filter part)

   Removes the unnecessary low frequency element contained in doppler signal by body movement, to receive signal of each channnel.

4. ADD (Adding part)

   Adds the received signals.

5. HIGH PASS FILTER (High frequency pass filter part)

   Removes the unnecessary low frequency element contained in doppler signal by body movement, for added receive signal.

6. GAIN (Gain process part)

   Amplifies or attenuates Doppler signal.

7. ANALOG WALL FILTER (High area pass filter part)

   Deletes unnecessary low frequency element which is mixed into Doppler signal by body movement.

8. ANTI ALIASING FILTER (Anti aliasing filter part)

   Deletes unnecessary high frequency element to prevent aliasing by A/D converter described later.

9. AD CONVERTER (AD convert part)

   Converts the added receive signal to digital signal and sends to EPI P.C.B.

10. CW CONTROL (CW control part)

    Controls the frequency setting for reference wave, the gain setting and other settings.

11. LO GENERATOR (Mixing clock generate part)

    Generates the clock of Mixer.

4.5 CW Doppler Unit EZU-CW4

4.5.1 General and board description

Composition : EZU-CW4 is an option of EUB-5500 and consists of the following PCB.

1. CW PCB

Outline of PCB : This is for CW Doppler by single piece probe, and carries out transmission and reception, demodulation and filter process of Doppler signal.

4.5.2 CW PCB circuit description

CW PCB is divided into the following 11 blocks.

1. REFERENCE CLOCK GENERATOR (Reference clock generation circuit part)

   Generates transmitting signal clock for CW and reference signal having 90 degrees different phase.

2. TRANSMITTING CIRCUIT (Transmission circuit part)

   Outputs transmitting signal clock for CW to the probe through tuning amplifier and driver circuits.

3. PRE AMP (First step amplification circuit part)

   Tunes and amplifies the receiving signal from the single piece prove.

4. NOTCH FILTER (Notch filter circuit part)

   Deletes the carrier element, which leak into the circuit, so that the receiving signal does not saturate with them.

5. MIXER (Demodulation circuit part)

   Detects the element of Doppler shift by mixing with the reference wave.

6. GAIN (Gain process part)

   Amplifies or attenuates Doppler signal.

7. ANALOG WALL FILTER (High area pass filter part)

   Deletes unnecessary low frequency element which is mixed into Doppler signal by body movement.

8. ANTI ALIASING FILTER (Anti aliasing filter part)

   Deletes unnecessary high frequency element to prevent aliasing by A/D converter described later.

9. AD CONVERTER (AD convert part)

   Converts the added receive signal to digital signal and sends to EPI P.C.B.

10. CW CONTROL (CW control part)

    Controls the frequency setting for reference wave, the gain setting and other settings.

11. LO GENERATOR (Mixing clock generate part)

    Generates the clock of Mixer.

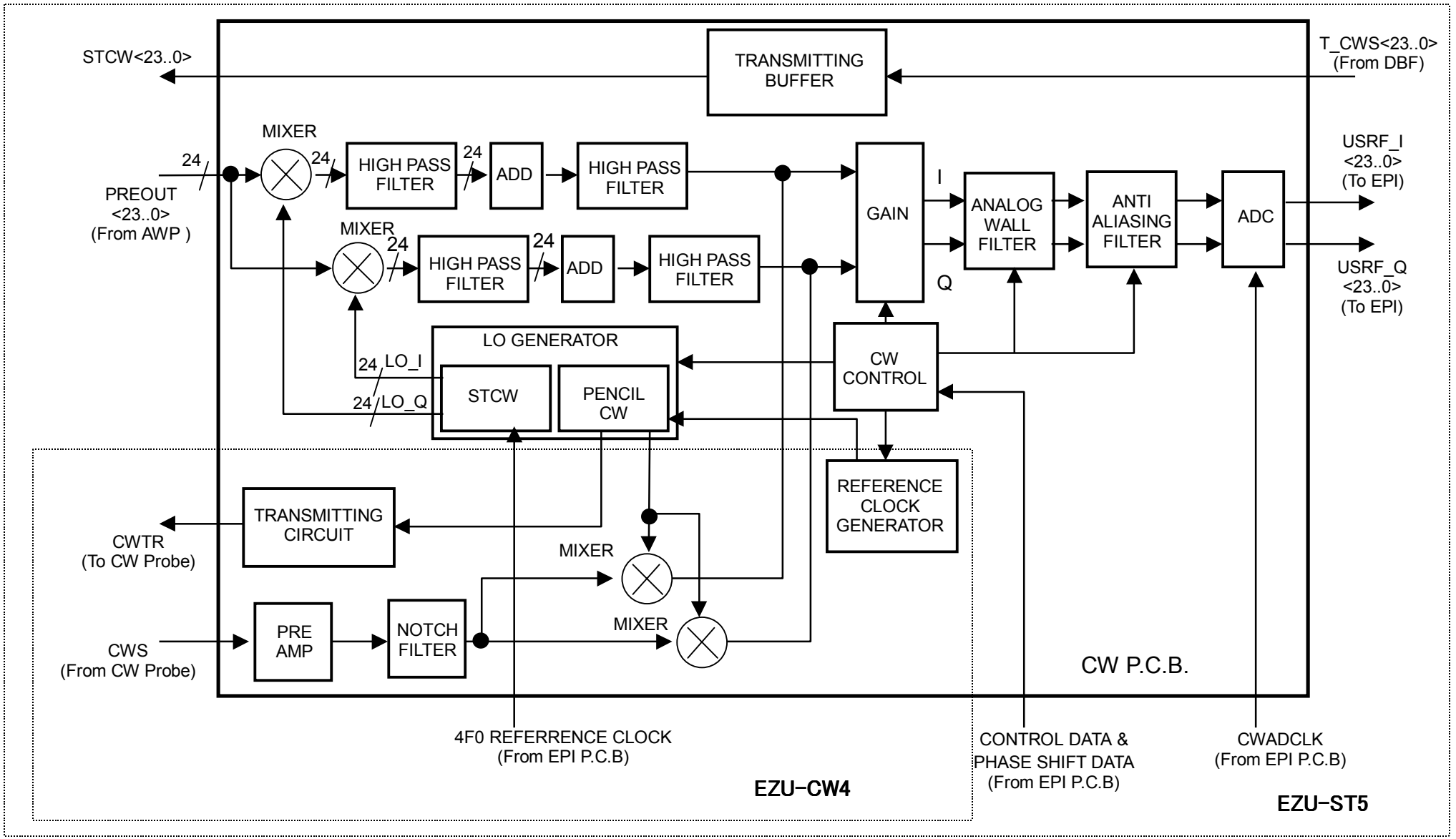


Fig. 4.5.1 EZU-ST5/CW4 Block Diagram

Section 5 Power Unit

5.1 General and Circuit Description

Composition: EUB-5500 power is composed of the following units.

1. HM-071C : Main power unit.
   HM-071K : DC-DC converter unit.

Power unit circuit description:

1. LINE FILTER (Line filter block)

   Removes noise on the AC line.

2. TRANS (Transformer block)

   Switches over voltage so that each circuit can operate in optimum voltage as well as isolates the primary and secondary circuits. A temperature fuse is built in the unit.(120℃)

3. PFC CIRCUIT (PFC circuit block)

   Consists of PFC circuit and protection circuit. The PFC circuit suppresses harmonics as well as improves distortion of voltage waveform and current wave height value to realize power-factor improvement.

   The protection circuit shuts off input by a signal from the overvoltage protection circuit.

4. MAIN CONVERTER CIRCUIT (Main converter circuit block)

   The switching conversion system converts power to voltage and supplies it to each DC converter via transformer.

5. RECTIFICATION AND SMOOTHING CIRCUIT (Rectification and smoothing circuit block)

   After rectifying by the diode, the power is smoothed by the capacitor to get DC source.

6. REGULATOR CIRCUIT (Regulation circuit block)

   The series type regulator system stabilizes DC output and reduces output ripples.

7. OVER CURRENT PROTECTION CIRCUIT (Overcurrent protection circuit block)

   When the load is short-circuited or overcurrent occurs, this circuit protects the load or power circuit.

8. OVER VOLTAGE PROTECTION CIRCUIT (Overvoltage protection circuit block)

   Protects the load and power circuit when output voltage exceeds over the rating.

9. Filter Circuit

   The noise from main converter is reduced by this circuit.

10 Chopper circuit

   This circuit provide stable DC output for digital circuit.

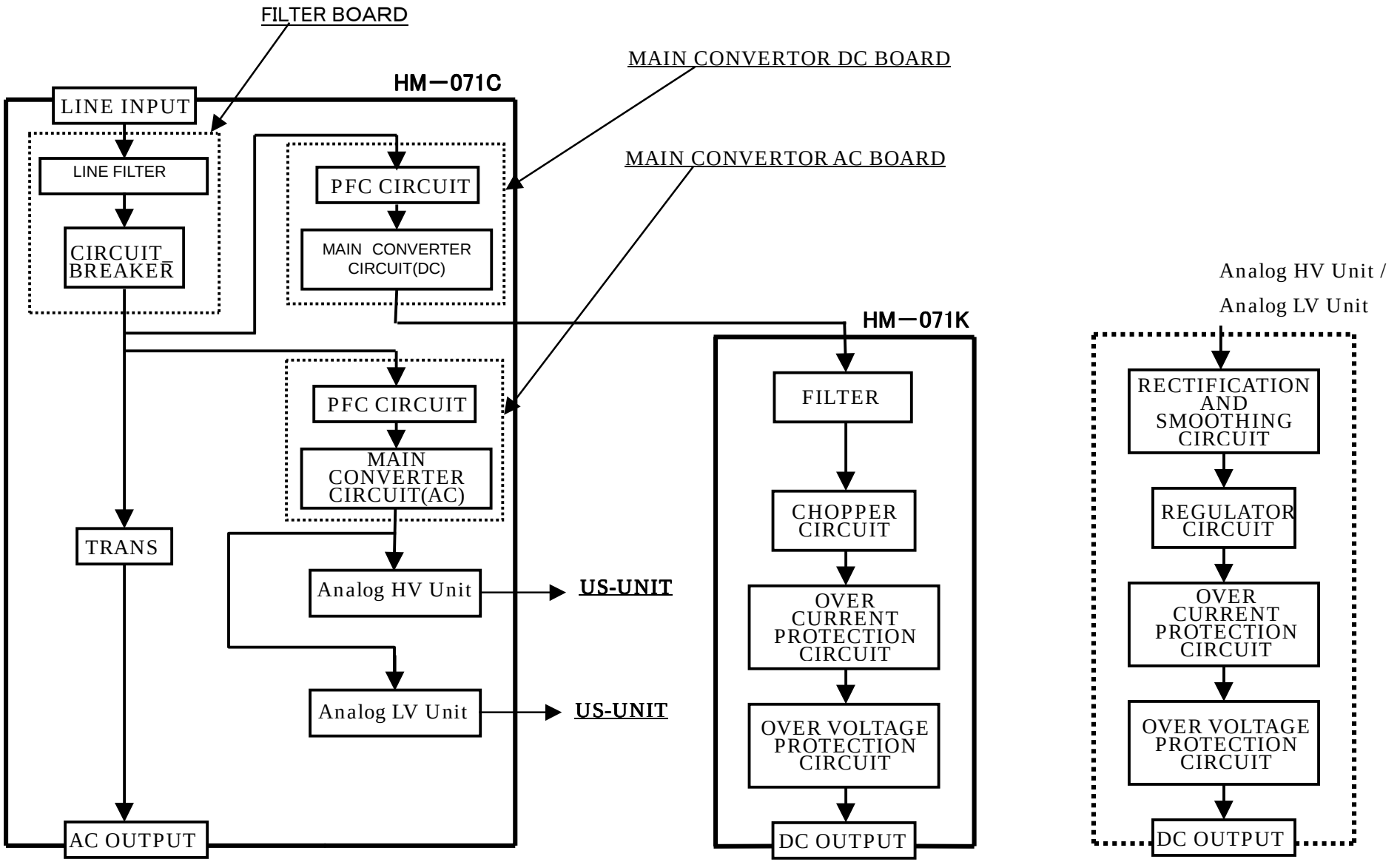


Fig5.1 POWER UNIT Block Diagram

5.2 Power Unit Connectors

HM-071C : CN1 : Connector for the circuit breaker.
CN2 : DC output connector for the analog unit (high-voltage).
CN3 : DC output connector for the analog unit (low-voltage).
CN4 : DC output connector for the digital unit.
CN5 : Connector to switch over AC input voltages.
NTSC system : AC100/110/120V can be switched over.
PAL system : AC220/230/240V can be switched over.
CN6 : AC output connector for the outlet.
CN7 : AC output connector for the monitor

HM-071K : PCB terminal connector : DC(+30V) input connector.
(DC output for the digital unit of HM-071C)
PCB terminal connector : DC output connector for the digital unit.

Connection specification:

HM-071C

Connector No.	Pin No.	Signal name	Remark
CN1	1	OUT L	Input of circuit breaker
	2	OUT N	
	3	IN L	Output of circuit breaker
	4	IN N	

Connector No.	Pin No.	Signal name	Output voltage	Remark
CN2	A1	+6.0	+6V	Output for AWP PCB
	A2	- 6.0	−6V	Output for AWP PCB
	A3	+12Vp	+12V	Output for PRB PCB and AWP PCB
	A4	- 12Vp	−12V	Output for AWP PCB
	A5	NC		
	A6	+75V	+75V	Output for AWP PCB
	A7	+75-GND		
	A8	+12Var	+4.5～+12V	Controlled by STVC (5bit) of CN3. Output for AWP PCB
	A9	−100V-GND		
	A10	- 100V	−100V	Output for PRB PCB
	B1	+6.0-GND		
	B2	−6.0-GND		
	B3	+12Vp-GND		
	B4	−12Vp-GND		
	B5	NC		
	B6	−75V	−75V	Output for AWP PCB
	B7	−75-GND		
	B8	+12Var-GND		
	B9	+100V-GND		
	B10	+100V	+100V	Output for PRB PCB

Connector No.	Pin No.	Signal name	Output voltage	Remark
CN3	A1	STVC0	−	Control signal of +12Var
	A2	STVC1		
	A3	STVC2		
	A4	NC		
	A5	+5Vc-GND		
	A6	+5Vc	+5V	Output for DBF PCB
	A7	−12Vb-GND		
	A8	−12Vb	−12V	Output for CW & DBF PCB
	B1	STVC3	−	Control signal of +12Var
	B2	STVC4		
	B3	GND(STVC)		
	B4	NC		
	B5	+5Vc-GND		
	B6	+5Vc	+5V	Output for DBF PCB
	B7	+12Vb-GND		
	B8	+12Vb	+12V	Output for CW & DBF PCB

Connector No.	Pin No.	Signal name	Output voltage	Remark
CN4	A1	+12V	+12V	Output for HM-071K
	B1	+12V-GND		
	A2、A3、B3	+30V	+30V	
	A4、B2、B4	+30V-GND		
	A5	+5VSB	+5V	Output for PC and HM-071K. Stand-by power of PC
	B5	GND		
	A6	P-CONT	—	
	B6	PROTECT	—	Protection signal

Connector No.	Input voltage	Connection
CN5	100Ⅴ/220V	A1-B2, A2-B1 short
	110Ⅴ/230V	A1-A3, A2-B1 short
	120Ⅴ/240V	A1-B3, A2-B1 short

Connector No.	Pin No.	Output voltage	Remark
CN6	1	0Ⅴ	For the AC outlet
	2	100Ⅴ/220V	
	3	110Ⅴ/230V	
	4	120Ⅴ/240V	
	5	GND	

Connector No.	Pin No.	Output voltage	Remark
CN７	1	0Ⅴ	For the monitor
	2	100Ⅴ	
	3	GND	

HM-071K

PCB terminal connector No.	Signal name	Output voltage	Remark	GND (PCB terminal connector)		
1a～1e 2a～2e	+12V-GND	-	Power for digital system (SELV system)	12a～12e 14a～14e 16a～16e 18a～18e 20a～20e ↓ 26a～26e 31a～31e ↓ 38a～38e 43a～43e ↓ 52a～52e 59a～59e ↓ 62a～62e 68a～68e ↓ 80a～80e 65a～65e ↓ 99a～99e 103a～103e ↓ 113a～113e ↓ 116a～116e		
3a～3e	+12V	-				
5a～5e ↓ 7a～7e	+30V-GND	-				
9a～9e ↓ 11a～11e	+30V	-				
13a～e	+5VSB	-				
15e	P-CONT	-				
17e	PW-OK	-				
19e	PROTECT	-				
27a～27e ↓ 29a～29e	+5Va	+5V				
39a～39e ↓ 41a～41e	+5Vb	+5V				
53a～53e ↓ 57a～57e	+2.5V	+2.5V				
63a～63e ↓ 66a～66e	+3.3Va	+3.3V				
81a～81e ↓ 83a～83e	+3.3Vb	-3.3V				
100a～100e 101a～101e	+12Va	+12V				
111a～111e	-12Va	-12V				

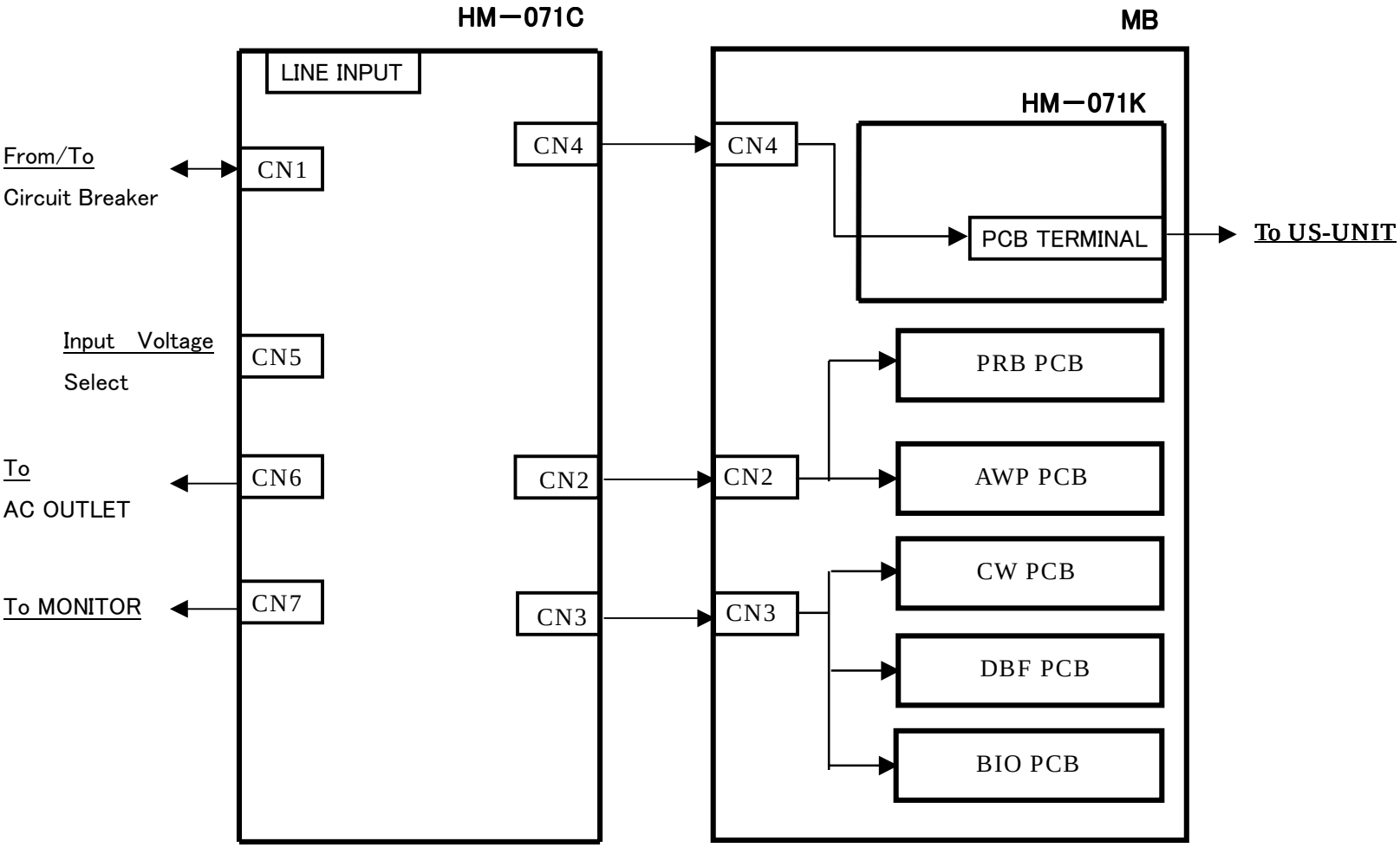


Fig5.2 POWER UNIT CONNECT Diagram

Table 5.1　Table of Power Supplies by Unit and PCB

		HM-071K(digital unit)								HM-071C(analog low-voltage unit)				HM-071C(analog high-voltage unit)								
		+2.5V	+3.3Va	+3.3Vb	+5VSB	+5Va	+5Vb	+12Va	−12Va	+5Vc	+12Vb	−12Vb	+12var	+5Vp	+12Vp	−12Vp	+6.0V	−6.0V	+75V	−75V	+100V	−100V
PC Unit	PC-MB			○	○	○		○	○													
	HD					○		○														
	VIDEO			○		○																
	FD					○		○														
	CD-R					○		○														
	EPI		○		○		○	○	○													
	MAP		○	○	○		○	○	○													
US Unit	PRB													○	○						○	○
	AWP												○	○	○	○	○	○	○	○		
	CW										○	○										
	DBF	○	○							○	○	○										
	BIO			○			○	○	○													
	KB						○															
Check point		DBF Contact 101A-E	EPI TP 3.3VIN (TP30)	MAP TP +3.3VIN	EPI TP +5VSB	PC-MB CN10 19, 20	EPI TP 5VIN (TP31)	EP TPI +12V	EPI TP −12V	DBF Contact 61A-E	DBF Contact 95A-E	DBF Contact 97A-E	AWP TP +12Var	AWP TP +5V	AWP TP +12V	AWP TP −12V	AWP TP +6V	AWP TP −6V	AWP TP +75V	AWP TP −75V	PRB C3	PRB C6

Section 6 Monitor Unit

6.1 Composition

The EUB-5500 monitor consists of the following unit.

EZU-MT24-S1

6.2 Specification

(1) Signal input impedance : 75Ω terminated

(2) Maximum gain : 32dB or more (with maximum contrast)

(3) Frequency characteristic : 60Hz ~ 30MHz (±3dB)
(When clicking the center of both contrast VR and brightness VR)

(4) Power input : AC100V±15% (50/60Hz)

(5) Power consumption : About 90VA

(6) Environmental requirements : Temperature 0 ~ 40ºC
Relative humidity 10 ~ 90% (No condensation)

(7) Weight : About 18kg

(8) Signal interface

a) Connector : Mini D-Sub 15-pin
b) Connections : See below:

Pin No.	Standard	When displaying external TV signal
1	Red Video signal	Red Video signal
2	Green Video signal	Green Video signal + sync signal
3	Blue Video signal	Blue Video signal
4	Standard←→External switching signal	Standard←→External switching signal
5	GND	GND
6	GND (Red)	GND (Red)
7	GND (Green)	GND (Green)
8	GND (Blue)	GND (Blue)
9	NC	NC
10	GND	GND
11	(Unused)	(Unused)
12	NC	NC
13	Horizontal sync signal	Horizontal sync signal
14	Vertical sync signal	Vertical sync signal
15	NC	NC

c) Standard←→External switchover signal : • Signal level TTL level
• Specification Standard : H level
External : L level

(9) Display : See below

	Standard		When displaying external TV signal	
	640×480	800×600	NTSC	PAL
Horizontal	260±4mm	258±4mm	260±4mm	257±4mm
Vertical	195±3mm	193.5±3mm	195±3mm	193±3mm

(10) Input signal level: See below. (Refer to Fig. 6.1.)

a) Standard

Input signal	Level	
	640×480	800×600
R	0.7Vp-p	
G	0.7Vp-p	
B	0.7Vp-p	
H-SYNC	TTL	
V-SYNC	TTL	

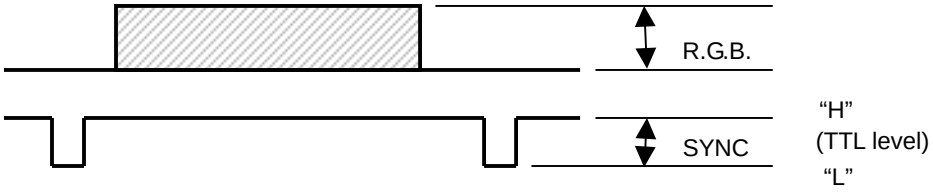
b) When displaying external TV signal

Input signal		Level	
		NTSC	PAL
R		0.716Vp-p	0.698Vp-p
G + SYNC	G	0.716Vp-p	0.698Vp-p
	SYNC	0.286Vp-p	0.301Vp-p
B		0.716Vp-p	0.698Vp-p

(11) Input signal timing: See below. (Refer to Fig. 6.2.)

Item		Formula	Standard		Displaying external TV signal		Unit
			640×480	800×600	NTSC	PAL	
a	Display time		25.94	25.76	52.04	51.52	µs
b	Blank time	c+d+e	5.84	6.24	11.50	12.48	µs
c	Front porch		0.38	1.06	1.78	1.76	µs
d	Pulse width of horizontal sync signal		3.92	3.32	4.70	4.68	µs
e	Back porch		1.54	1.86	5.02	6.04	µs
f	Cycle of horizontal sync signal	a+b	31.78	32.00	63.54	64.00	µs
g	Frequency of horizontal sync signal	1/f	31.47	31.25	15.735	15.625	kHz
h	Display time		(480H)	(600H)	(240H)	(289H)	ms
i	Blank time	j+k+l	(45H)	(25H)	(22H)	(25H)	ms
j	Front porch		(10H)	(1H)	(4H)	(3H)	ms
k	Pulse width of vertical sync signal		(2H)	(3H)	(3H)	(3H)	ms
l	Back porch		(33H)	(21H)	(15H)	(19H)	ms
m	Cycle of vertical sync signal	h+i	(525H)	(625H)	(262H)	(314H)	ms
n	Frequency of vertical sync signal	1/m	59.94	50.00	60	50	Hz
Scan system			Non-interlaced	Non-interlaced	Interlaced	Interlaced	—

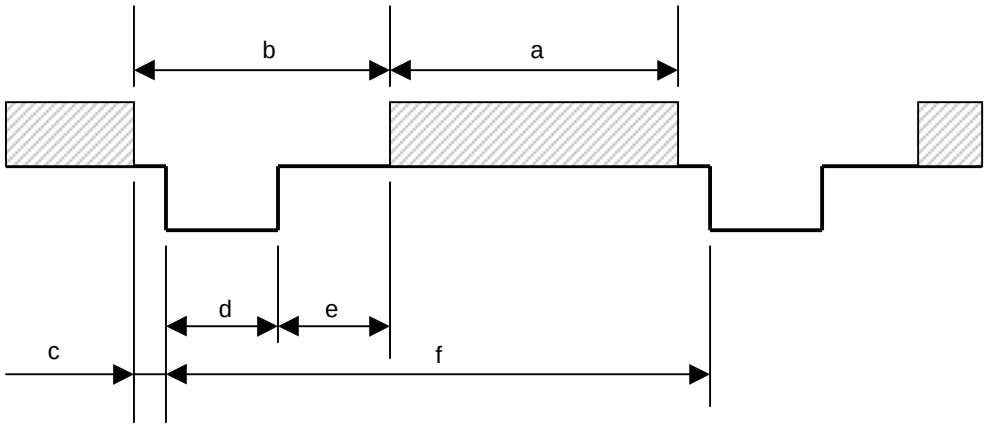
Standard



Displaying external TV signal

Fig. 6.1 Input Signal Level

HORIZONTAL



VERTICAL

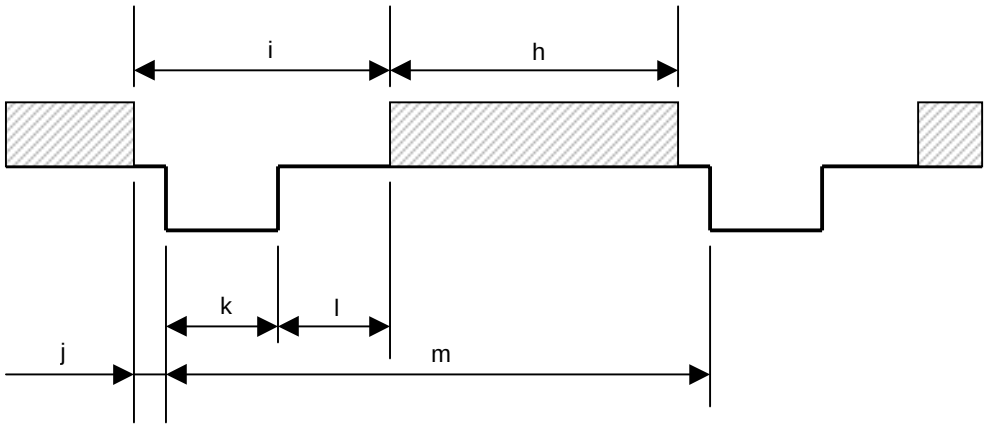


Fig. 6.2 Input Signal Timing

6.3 Installation

6.3.1 Cautions in installing the monitor

Convergence of the color monitor is affected from external induction magnetic field. Avoid installing the equipment in any region where induction magnetic field exists. Also observe the following cautions to obtain stable performance for a long period of time.

(1) Ventilation

To obtain stable performance for a long period of time, keep temperature inside the cabinet below 50ºC.

Especially fully ventilate in the vertical direction.

(2) Leakage magnetic field

Do not install the monitor in any region near the transformer, fan or the other leakage magnetic field sources as far as possible. Alternating current leakage magnetic flux causes fluctuation of images, and direct current magnetic flux (magnet or the like) causes raster distortion or degradation of image color purity. If it is necessary to install this equipment in such environment, satisfy the following conditions.

That is, for the transformer, attach the shielding ring and shorting ring to minimize leakage flux and design its winding of a balanced type. For devices other than the transformer, use magnetic shielding or non-inductive winding to minimize leakage magnetic flux. Effect to the monitor may appear in a magnetic field of 0.01 Gauss or more.

(3) Humidity

This monitor may be operated in a range of 10~90% relative humidity; however, it is recommended to operate it in a range of 30~70% relative humidity since life of connecting points of connectors, switches, variable resistors, etc. could become shorter.

(4) Ambient illumination

This monitor uses the black matrix tube showing excellent performance against glare or reflection in a bright room.

However, to reduce fatigue of operator's eyes, install it so as to avoid any light source that may directly illuminate the tube face of CRT.

(5) Dust

This monitor has been designed to minimize accumulation of dust; however, high static electric field extracts dust through the ventilation holes of cabinet. Therefore, take care to minimize dust around the monitor.

(6) Power supply voltage

This monitor is built in with the voltage stabilizer circuit, so images are not affected from voltage fluctuation within the specification.

However, avoid operation exceeding ±10% to prevent excessive heat inside the monitor and reduced life of the monitor.

Either of 50Hz and 60Hz can be used without modification of the equipment.

(7) Dust on CRT face

Applied high voltage has tendency to collect dust on the tube face of CRT, and it deteriorates brightness and focusing quality.

To remove this dust periodically, use soft cloth moistened with silicone type glass cleaner. Never use thinner or the like instead of the cleaner.

6.3.2 Cautions for safety

NOTE: Observe all the cautions and notices concerning safety labeled on the chassis or CRT.

(1) Hazardous voltage exists in the monitor. When removing the cover to work in the equipment, be sure to observe general electrical cautions.

(2) Before removing or replacing PCB (module) and parts, turn OFF the power.

(3) Residual charge may remain in the anode cap. Greatest care should be taken for replacement or inspection maintenance of CRT.

(4) Do not replace any parts at your discretion. Fire, X-ray or other hazard may result.

6.3.3 Replacing the fuse

When the fuse is to be replaced, use that supplemented to the monitor or the same type and capacity.

The fuse is mounted on the main board (AVB401) inside the monitor. Be sure to turn OFF the power before removing the cover and replacing the fuse.

6.3.4 Degaussing

This monitor is equipped with the automatic and manual degaussing function.

When turning ON the power, it is automatically degaussed. If the monitor is magnetized in any reason and color purity of the image is deteriorated, remove the cover and press the DEGAUSS switch on the VIDEO board (AVB411) to manually degauss.

If this action cannot fully degauss the monitor, use the degaussing coil commercially available to do so externally.

6.4 Description of Operation

6.4.1 General

This monitor is composed roughly of the following 6 modules:

① Brown tube
② Main board
③ VIDEO board
④ Socket board
⑤ Control board
⑥ Front control board

6.4.2 Brown tube (CRT)

CRT is designed to make a light spot on the fluorescent screen by electron beam emitted from the electron gun, deflect the electron beam with the deflection coil in a constant cycle, and display an image by a locus of this light spot.

CRT is composed of the fluorescent screen coated in three colors, shadow mask and electron gun to emit three electron beams. The electron gun is composed of metal coil heater, cathode and grid arranged on a line.

The 3-beam electron gun is arranged in line, so section of three electron beams is arranged in line horizontally.

Three electron beams emitted from the electron gun are deflected to scan whole fluorescent screen. Electron beam is blocked off by the shadow mask and hits fluorescent material only corresponding to each color when it passes through the hole.

A set of dots emits light of red, green and blue depending on color signal intensity to reproduce every possible color.

6.4.3 Main board (AVB401)

The main board is composed of the following:

① Power supply circuit
② Horizontal deflection and high voltage circuit
③ Vertical deflection circuit

6.4.3.1 Power supply circuit

(1) Main circuit

Input voltage is supplied via the filter and rush current limit circuit. This is rectified and smoothed by the rectifier diode (D100) and input capacitor (C103) to obtain DC coarse rectified voltage. This is switched by the main transistor (Q101) and transformer (T100) to produce each voltage of P120 (+120V), P70 (+70V), P24 (+24V), P12 (+12V), HEATER (+6.3V) and P5 (+5V).

(2) Control circuit

P120 output voltage is compared with the reference voltage by the detector circuit. Signal from the detector circuit is fed back to the control circuit via the photo-coupler (PC100).

The control circuit controls ON time of the main transistor (Q101) to generate appropriate drive pulse to stabilize the output P120. Switching frequency is controlled so as to synchronize with the horizontal deflection signal.

(3) Overvoltage and overcurrent protection

In case of overvoltage and overcurrent, this protection circuit keeps the state by IC800 when switching of Q101 stops. To restart it, turn OFF the power for 30 seconds or more and turn ON again.

(4) +B power circuit

The +B power circuit controls +B voltage including SPCC and horizontal size adjustment function. Output is adjusted by VR101 (for TV timing) and VR102 (for PC timing) and stabilized by the control circuit (IC106) and switching of the transistor (Q122). Switching frequency is controlled so as to synchronize with horizontal deflection signal.

6.4.3.2 Horizontal deflection and high voltage circuits

In the horizontal and high voltage drive circuit, horizontal AFC circuit IC110 and drive transistor Q119 drive the deflection coil to flow the horizontal deflection current, and also drive the flyback transformer (FBT) to supply high voltage of about 24kV to the anode of CRT.

High voltage is adjusted by VR105, and stabilized by switching of transistor (Q120) and control circuit (IC108).

If high voltage increases abnormally in any trouble, the high voltage protection circuit (IC107) controls high voltage to reduce +B voltage, and stops switching of the horizontal AFC circuit (IC110) to stop output. To release stop of the protection mode, the power needs to be turned OFF and then ON.

6.4.3.3 Vertical deflection circuit

In the vertical deflection circuit, the vertical oscillation circuit (IC110) and the drive circuit (IC109) drive the deflection coil to flow vertical deflection current.

6.4.4 VIDEO board (AVB411)

The VIDEO board is consists of the following circuits:

① Amplifiers for each channel of red, green and blue (VIDEO Amp)
② Sync separation circuit
③ NTSC/PAL signal detection circuit
④ Degauss control circuit

6.4.4.1 VIDEO Amp

(1) Image preamplifier circuit
Image input signal is supplied to the input of image preamplifier (IC300) via the AC coupling capacitors (C318, C320 and C317).

(2) Contrast control and image post-amplifier circuit
Varying bias voltage of 24-pin of IC300 controls contrast.

Red (VR304), green (VR305) and blue (VR306) adjust gain of image amplifier channels for a white balance of image.

Also VR308 adjusts brightness of the contrast center.

IC304 is a final stage of image amplifier to output a signal to the cathode of CRT via the red (Q303, Q304), green (Q305, Q306) and blue (Q307, Q308).

(3) Bias control
The red (Q303, Q304), green (Q305, Q306) and blue (Q307, Q308) controls DC bias to control brightness and white balance of raster.

The red (VR302), green (VR301) and blue (VR300) adjust white balance, while VR303 adjusts brightness of the brightness center.

6.4.4.2 Sync separation circuit

IC305 automatically separates H. SYNC and V. SYNC for following 3 modes of sync signal input:

① Composite sync
② H /V mixed sync
③ H /V separated sync

IC305 also generates a cramp pulse in the horizontal back porch period to regenerate DC level of the image circuit.

6.4.4.3 NTSC/PAL signal detection circuit

Converts frequency of NTSC (fv: 60Hz) and PAL (fv: 50Hz) to voltage by the F/V converter (IC301), and compares the voltage by the comparator (IC302) to output switchover signals.

6.4.4.4 Degauss control circuit

The degauss switch is a momentary type. Once it is pressed, degaussing is kept for about 10 seconds. It needs not to press continuously.

Also, when turning ON the power, degaussing is automatically effected.

6.4.5 Socket board (AVB421)

This board is mounted with CRT socket and supplies image signal, heater voltage, 1st and 2nd grid voltage and focus voltage to CRT.

6.4.6 Control board (AVB451)

Depending on each timing switchover signal, adjustment variable resistors are switched over as shown in Table below.

Once it is set, images of respective timing can be displayed without readjustment.

Name	Timing			
	640×480	800×600	NTSC	PAL
HEIGHT	VR21	VR20	VR19	VR18
H-PHASE	VR17	VR16	VR15	VR14
V-CENT	VR13	VR12	VR11	VR10

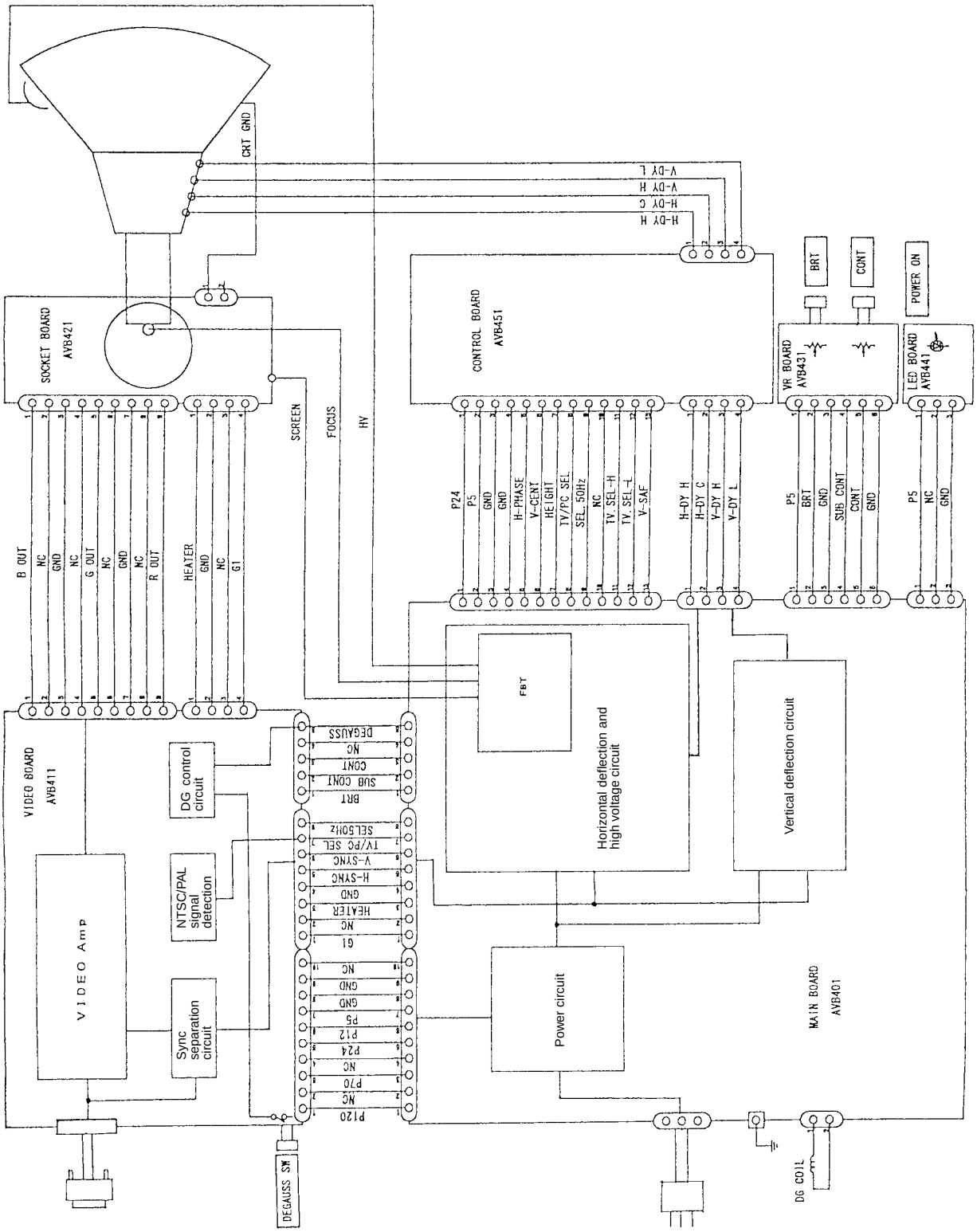
6.4.7 Front control (AVB431)

The front control includes the brightness and contrast variable resistors.

The brightness variable resistor adjusts brightness of raster, while the contrast variable resistor adjusts brightness of image.

Either variable resistor is provided with the center click to obtain standard brightness when centered.

6.4.8 Block diagram



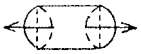
6.5 Adjustment

6.5.1 List of adjusters

(1) Front controller (AVB431)

No.	Name		Function	Polarity (clockwise)	Position	Remarks
	Device No.	Symbol				
1	VR1	BRIGHTNESS VR	Brightness of back raster	Brighter	Front	With center click (Center default)
2	VR2	CONTRAST VR	Brightness of image	Brighter	Front	With center click (Center default)

(2) Main board

No.	Name		Function	Polarity (clockwise)	Position	Remarks
	Device No.	Symbol				
1	VR100	P120	DC output voltage	Higher voltage	Upper	Unchangeable
2	VR101	WIDTH 1	Horizontal screen size (For TV timing)	Wider	Upper	
3	VR102	WIDTH 2	Horizontal screen size (For PC timing)	Wider	Upper	
4	VR103	TRIP (HV TRIP)	High voltage trip point to protect abnormal high voltage	Higher	Upper	Unchangeable
5	VR104	SPC	Correction of side pinction		Upper	
6	VR105	HV ADJ	High voltage (Anode voltage)	Higher	Upper	Unchangeable
7	VR106	H-HOLD	Horizontal frequency sync	Higher frequency	Upper	Unchangeable
8	FBT	FOCUS	Focus	—	Side	
9	FBT	SCREEN (VG2)	Screen voltage (VG2)	Brighter	Side	

(3) VIDEO board (AVB411)

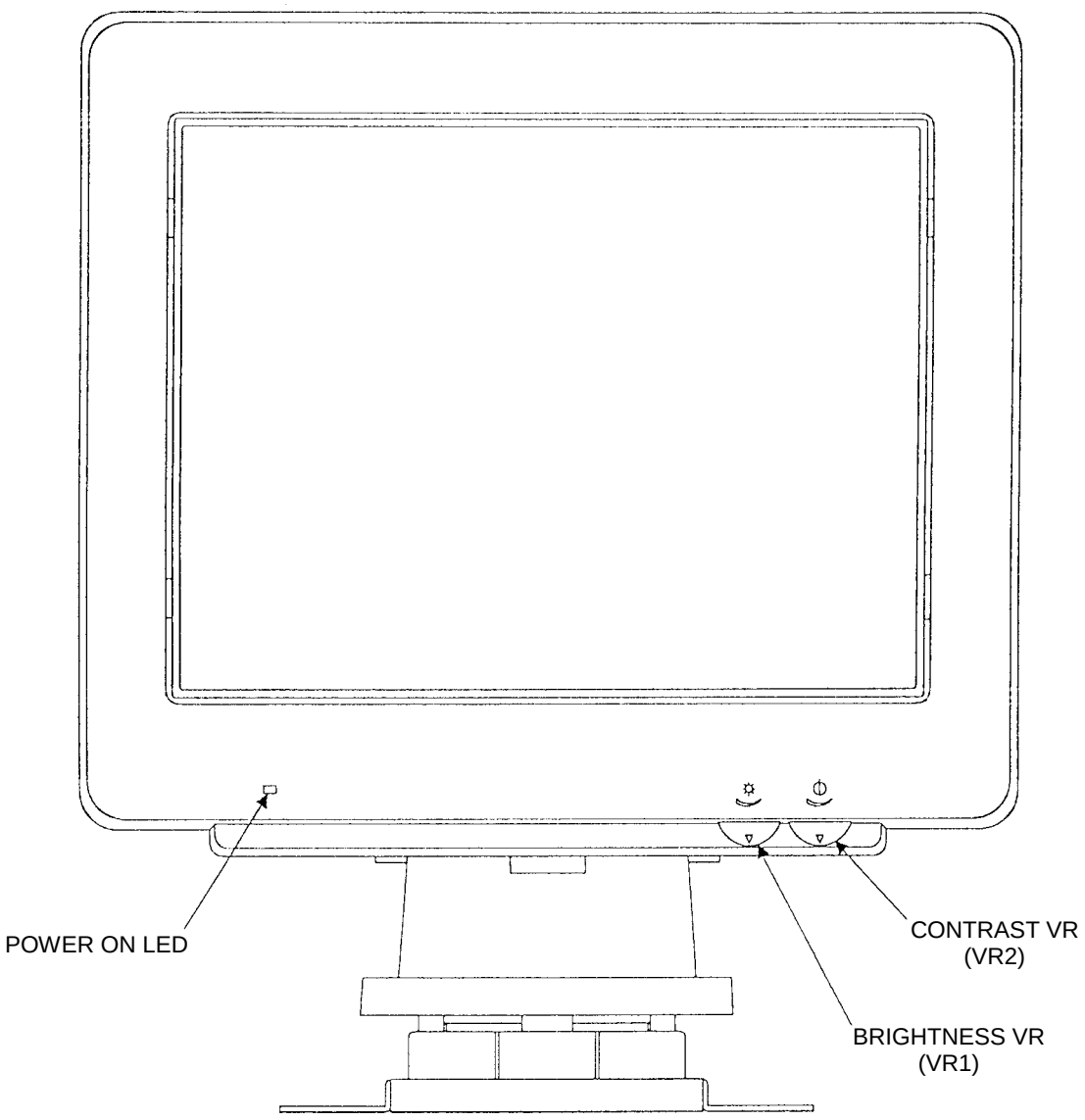
No.	Name		Function	Polarity (clockwise)	Position	Remarks
	Device No.	Symbol				
1	VR300	B CUT OFF	White balance of back raster	Raises blue level	Rear	
2	VR301	G CUT OFF		Raises green level	Rear	
3	VR302	R CUT OFF		Raises red level	Rear	
4	VR303	SUB BRT (SUB BRIGHTNESS)	Rated brightness of back raster	Darker	Rear	
5	VR304	R DRIV	White balance of image	Lowers red level	Rear	
6	VR305	G DRIV		lowers green level	Rear	
7	VR306	R DRIV		Lowers blue level	Rear	
8	VR307	F/V ADJ	Output voltage of F/V converter	—	Rear	Unchangeable
9	VR308	SUB CONT (SUB CONTRAST)	Rated brightness of image	Brighter	Rear	
10	SW300	DEGAUSS SW	Manual degauss function (for better color purity)	Press to ON (Non-lock)	Rear	

(4) Control board (AVB451)

No.	Name		Function	Polarity (clockwise)	Position	Remarks
	Device No.	Symbol				
1	VR10	V-CENT	Vertical screen position	Lower	Side	PAL timing
2	VR11			Lower	Side	NTSC timing
3	VR12			Lower	Side	800×600 timing
4	VR13			Lower	Side	640×480 timing
5	VR14	H-PHASE	Horizontal screen position	To the left	Side	PAL timing
6	VR15			To the left	Side	NTSC timing
7	VR16			To the left	Side	800×600 timing
8	VR17			To the left	Side	640×480 timing
9	VR18	HEIGHT	Vertical screen size	Wider	Side	PAL timing
10	VR19			Wider	Side	NTSC timing
11	VR20			Wider	Side	800×600 timing
12	VR21			Wider	Side	640×480 timing

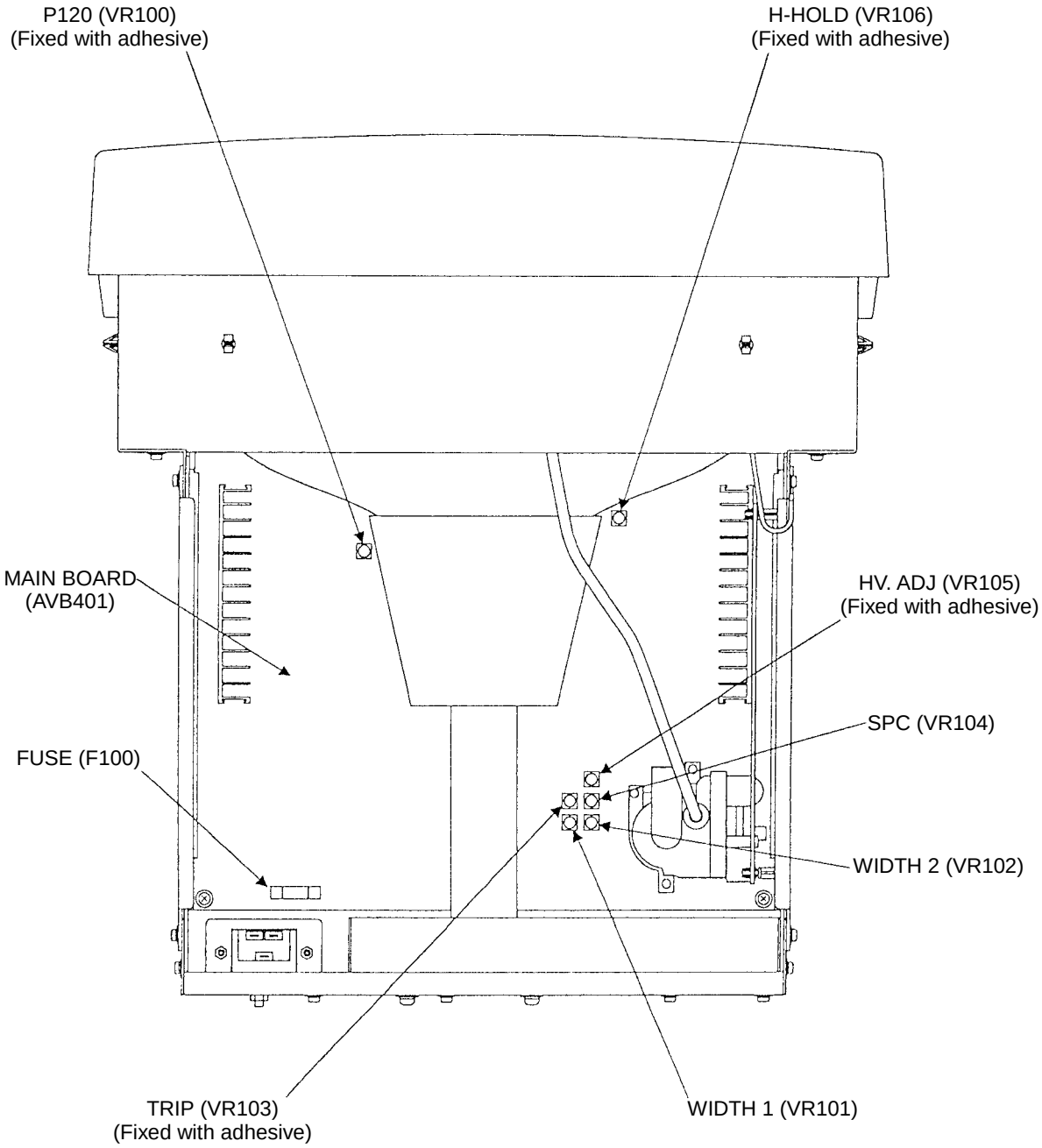
6.5.2 VR adjuster layout

(1) Front controls



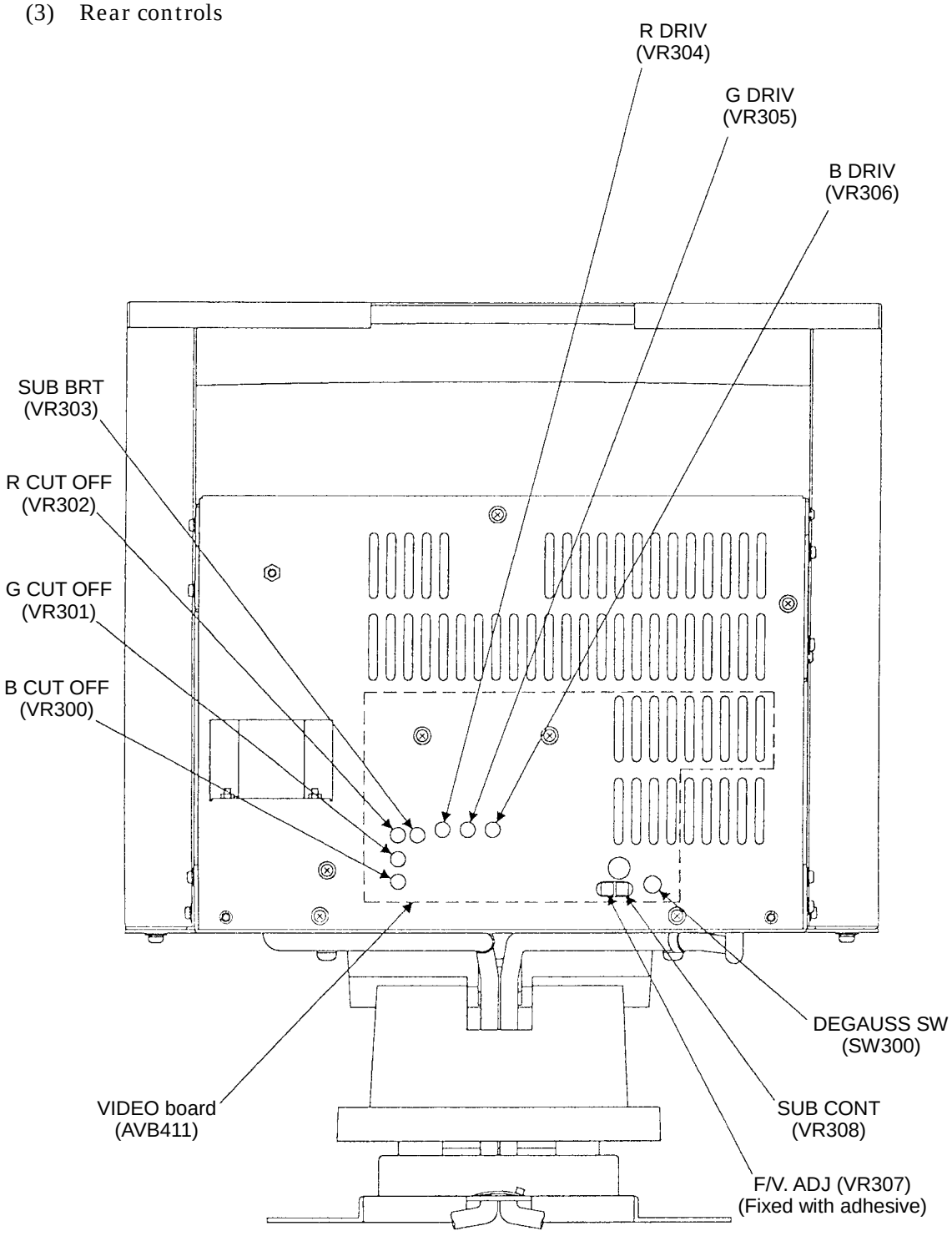
Layout of Front Control VR

(2) Upper controls



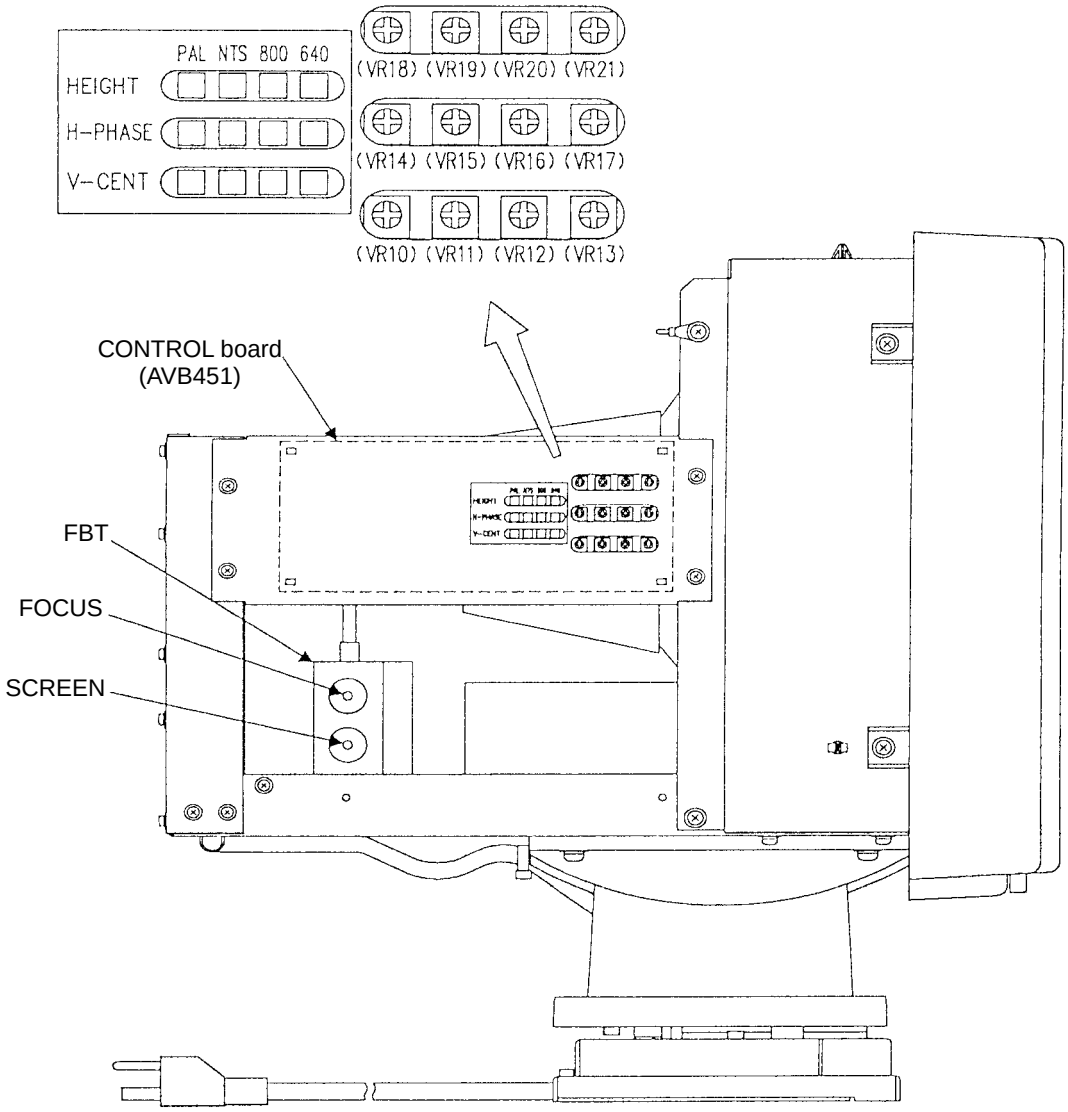
Layout of Upper Control VR

(3) Rear controls



Layout of Rear Control VR

(4) Side controls



Layout of Side Control VR

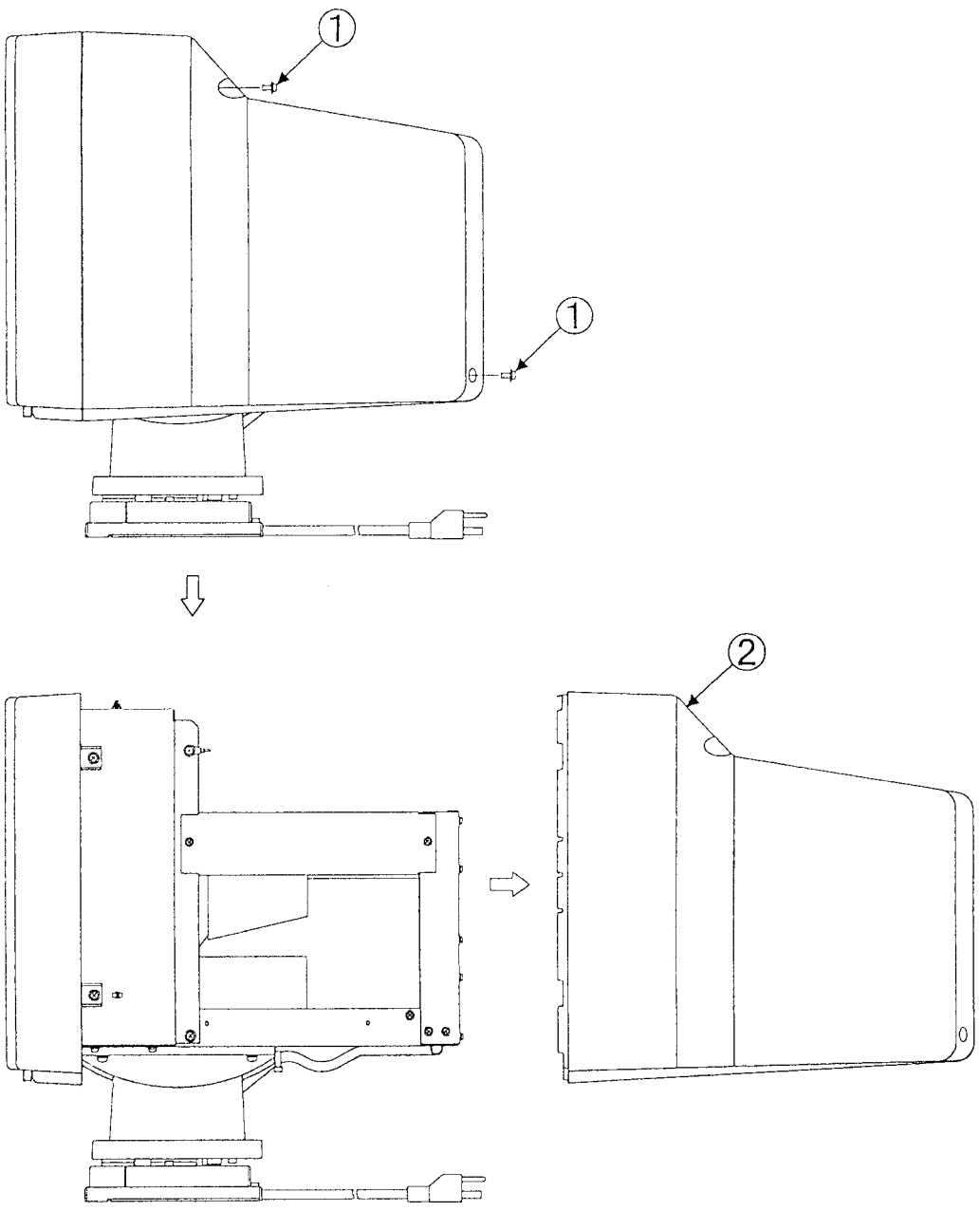
6.6 Troubleshooting

Troubleshooting

- Find any failure from the column below.
- Follow along the line to the right where marked with "○" and then follow upward to find suspected cause and action to be taken described in the upper columns.

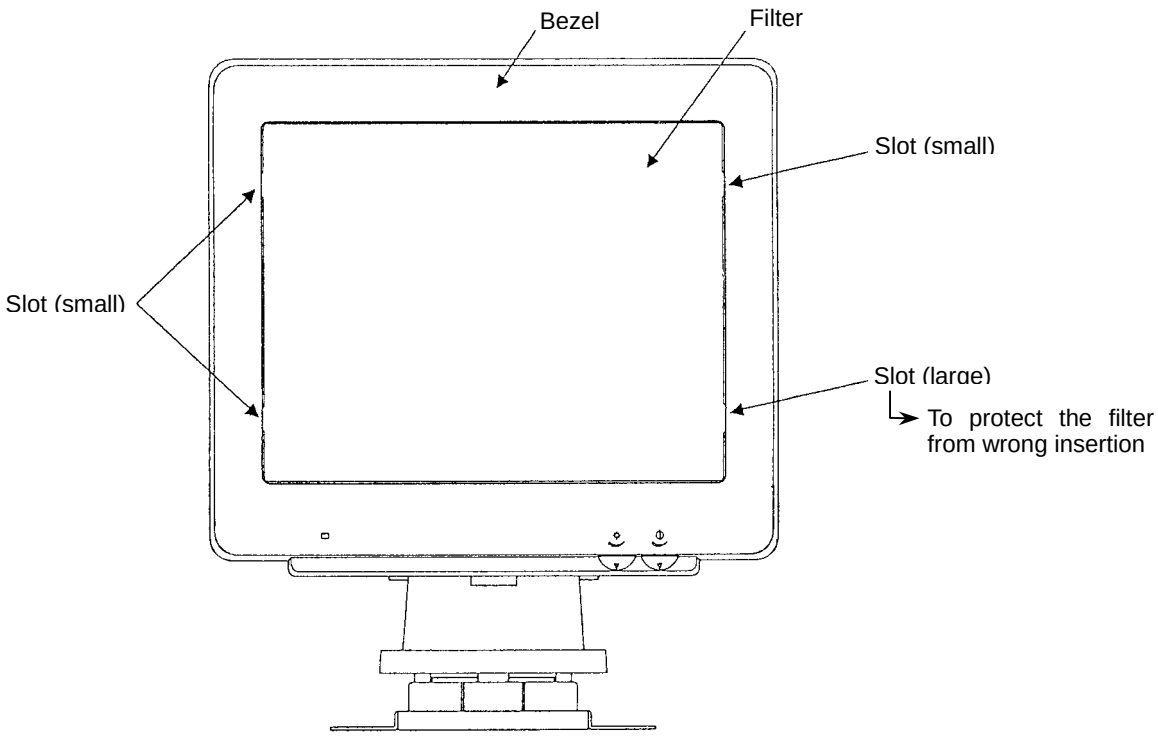
Item	Installation			Protection and adjustment function			Internal adjustment	Failure					
Suspected cause	Faulty connection of signal cable	Mismatch of signal interface (Level, timing)	Effect from magnetic field of the other monitor, etc.	Fuse is blown out.	Overload protection due to temporary noise.	Contrast and brightness VR are set to the minimum.	Adjustment is not correct.	Main board (AVB401)	VIDEO board (AVB411)	Socket board (AVB411)	CRT (with deflection yoke)	Control board (AVB451)	Front control (AVB431)
Action	Connect correctly.	Add rated waveform.	Keep clear of magnetic source.	Put in the rated fuse.	Turn OFF the power switch and wait for 1 min then turn ON again.	Set them in the optimum range	Refer to description in each column to retry adjustment.	Replace the module.					
Image quality													
The screen rotates, missing sync.	○	○						○	○			○	
Too narrow screen width		○					WIDTH 1, 2 VR (VR101, 102)	○				○	
Too wide screen width		○					WIDTH 1, 2 VR (VR101, 102)	○				○	
Too small screen height		○					HEIGHT VR (VR18~21)	○				○	
Too large screen height		○					HEIGHT VR (VR18~21)	○				○	
The screen is not at the center.		○					H-PHASE VR (VR14~17)	○				○	
Ditto		○					V-CENTER VR (VR10~13)	○				○	
The screen is too dark.	○	○				○		○	○	○	○		○
The screen is too bright.	○	○				○		○	○	○	○		○
White balance is bad.		○					Adjust white balance.		○				
Any of 3 color beams is missing.							Adjust white balance.		○	○	○		
Color purity of white is bad.		○	○			○	Degauss switch		○	○	○		
Image is not sharp (bad focusing).		○				○	Adjust focusing.	○	○	○	○		
No image appears.					○	○	Adjust contrast and brightness.	○	○			○	○
Overshoot and smear appear.	○	○							○				
Noise on the screen.	○				○			○	○				
The power indicator does not light.				○	○			○					
Color varies if brightness varies	○	○	○				Adjust white balance.	○	○	○	○		
Arc in CRT								○			○		

6.7 Removing the Cover



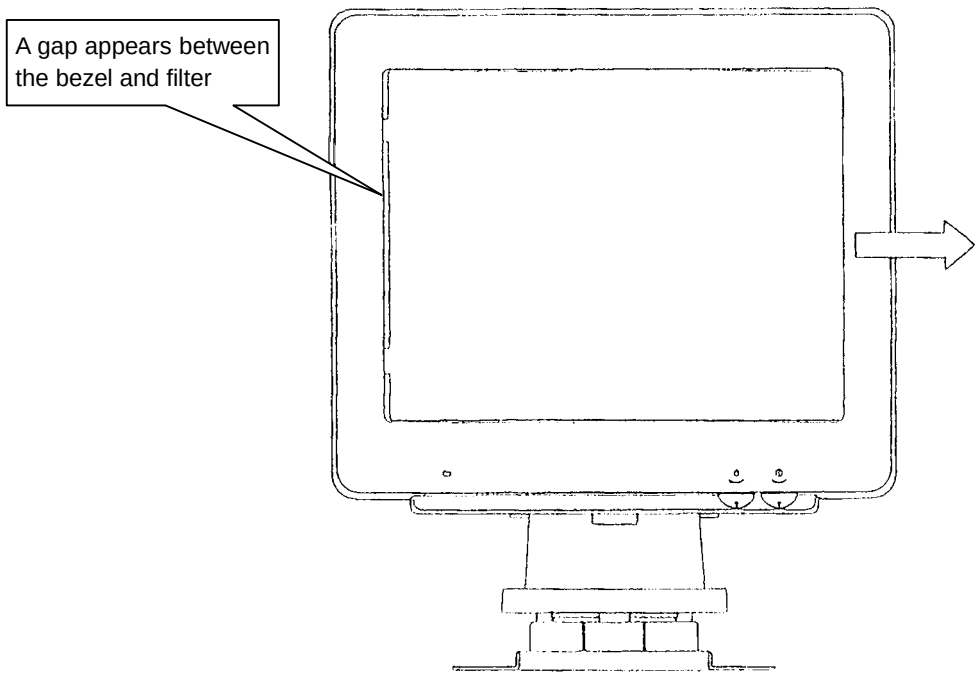
1) Remove M4×10 screws ① (4 locations).
2) Withdraw the cover② backward to detach it.

6.8 Detaching and Attaching the Filter

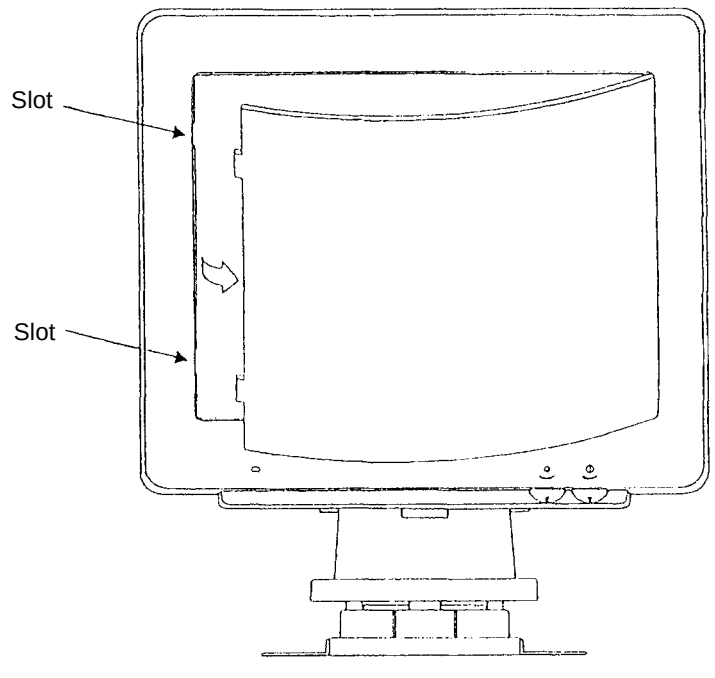


6.8.1 Detaching the filter

(1) Slide the filter to the right



(2) While curving the filter, take the projections (2 locations) at the right side of filter out of the slots of bezel to detach the filter.

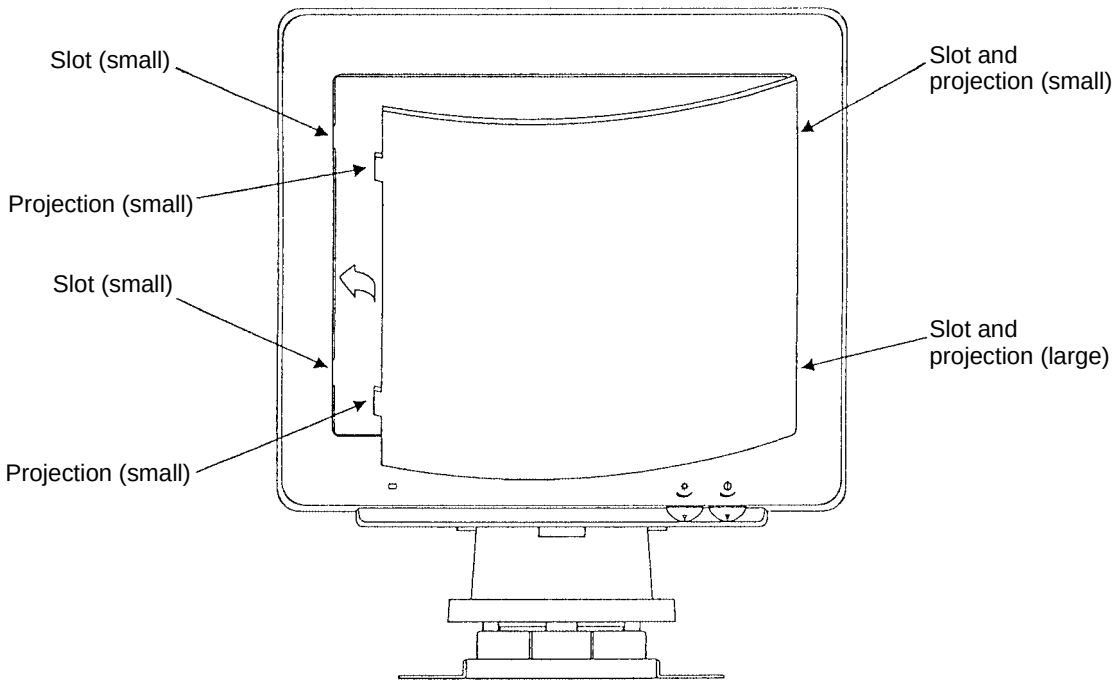


6.8.2 Attaching the filter

(1) Set the filter so that the projections of filter (large) come to the lower right facing to the bezel.

(2) Insert the projections into the slots at the right side facing to the bezel.

(3) Curve the filter and fit the projections into the slots at the left side of bezel.

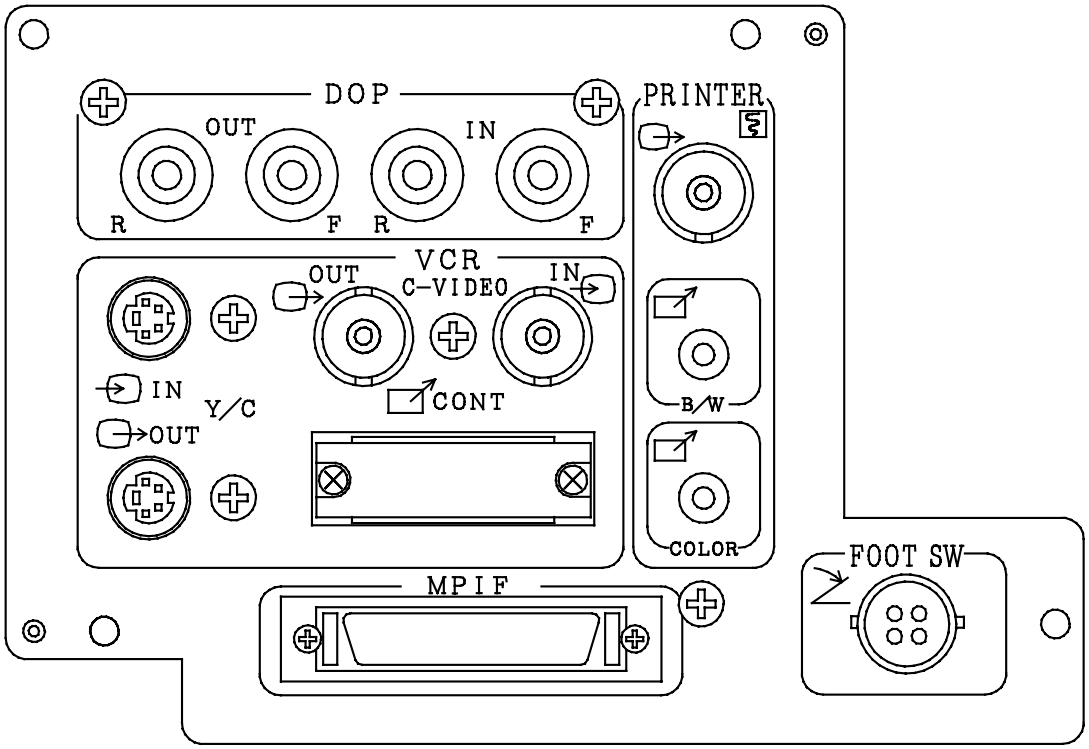


Section 7 Connector Arrangement

7.1 Connector Arrangement

Fig 7.1.1 shows external appearance of the CN panel.

Fig 7.1.2 shows connector arrangement of the overall system.



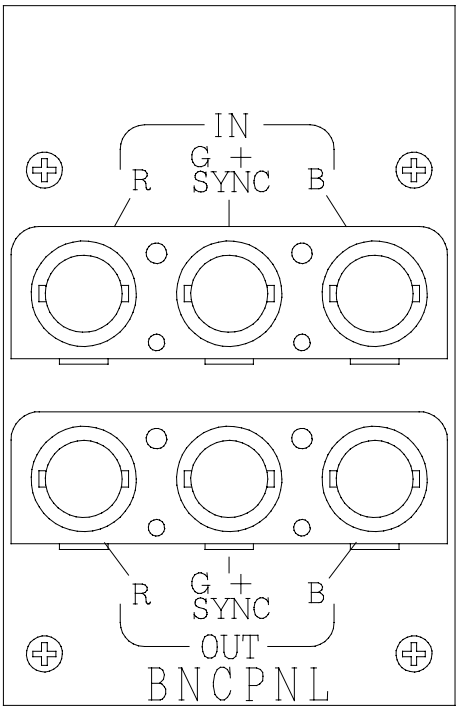


Fig 7.1.1 CN panel

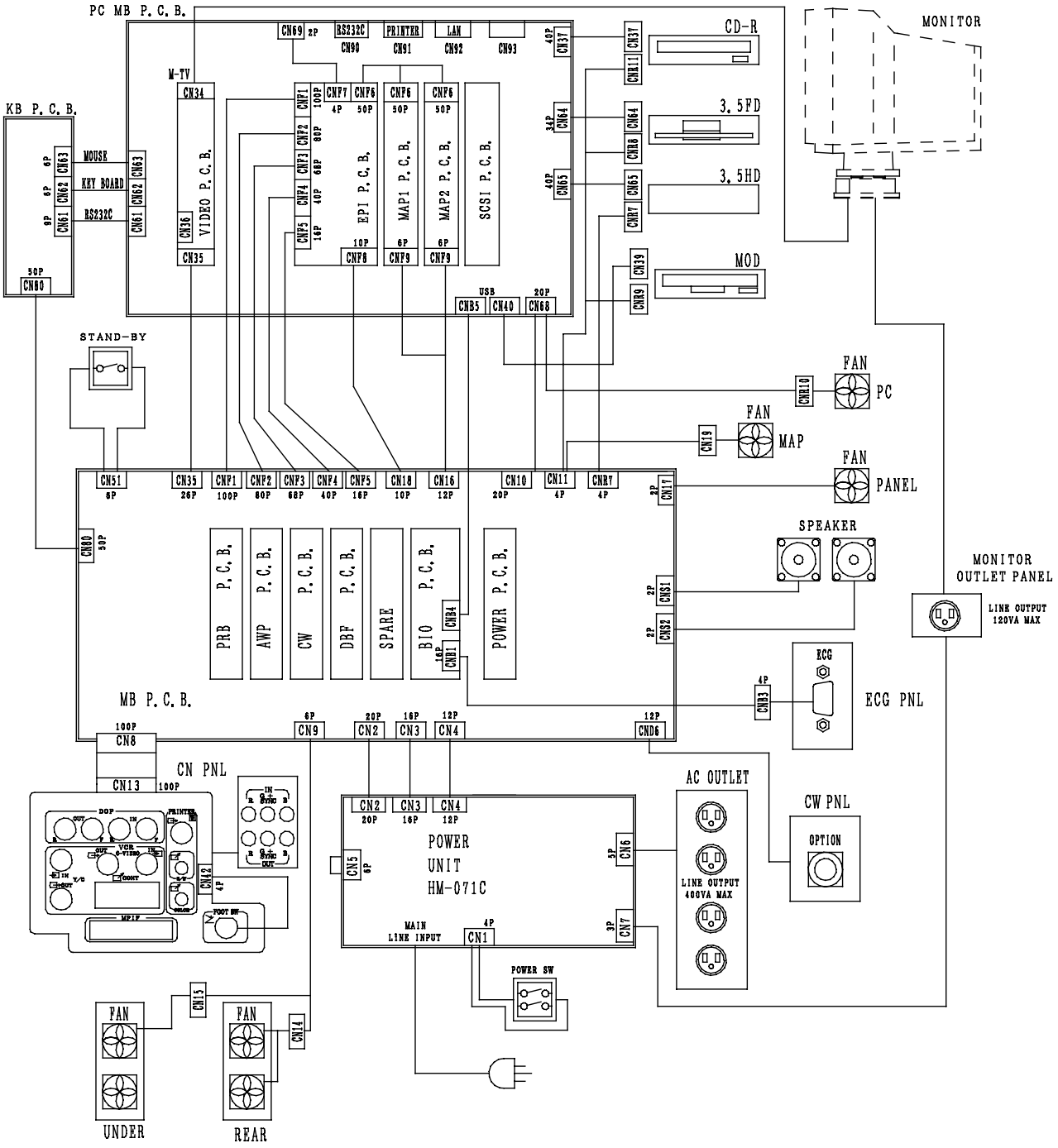


Fig 7.1.2 Connector arrangement

7.2 Connection of CN panel connector

CN No.	PIN No.	Signal Name	From/To	Remark
CN42	1	F-FREEZE	To KBIF	FOOT SW
	2	F-SHUTTER		
	3	GND		
	4	GND		

CN No.	PIN No.	Signal Name	From/To	Remark
CN13	1	GND		
	2	F-FREEZE	To KBIF	FOOT SW
	3	F-SHUTTER		
	4	GND		
	5	GND		
	6	FWD	From EPI	DOP out F
	7	REV		DOP out R
	8	GND		
	9	GND		
	10	VCR_FWD	To EPI	DOP in F
	11	VCR_REV		DOP in R
	12	B_OUT	From VIDEO	RGB-VIDEO OUT(B)
	13	G_OUT		RGB-VIDEO OUT(G-sync)
	14	VBSOUT	From VIDEO	C-VIDEO OUT
	15	BWOUT		C-VIDEO
	16	R_IN	To VIDEO	RGB-VIDEO IN(R)
	17	R_OUT	From VIDEO	RGB-VIDEO OUT(R)
	18	COUT	From VIDEO	Y/C-OUT
	19	YOUT		
	20	G_IN	To VIDEO	RGB-VIDEO IN(G-sync)
	21	GND		
	22	VBSIN	To VIDEO	C-VIDEO IN
	23	GND		
	24	B_IN	To VIDEO	RGB-VIDEO IN(B)
	25	GND		
	26	CIN	To VIDEO	Y/C-IN
	27	YIN		
	28	GND		
	29	GND		
	30	GND		
	31	GND		
	32	SP_AMODE_G	From DBF	SP-711UA control
	33	SP_AMODE		
	34	SP_AMODE_G		
	35	GND		
	36	SP_GAIN_G	From DBF	
	37	GND		
	38	SP_GAIN	From DBF	
	39	GND		
	40	SP_GAIN_G	From DBF	
	41	SP_USTRIG		
	42	SP_USTRIG_G		
	43	GND		
	44	SP_USTRIG_G	From DBF	
	45	GND		
	46	GND		
	47	SP_SPARE21	Not used	
	48	GND		
	49	GND		
	50	SP_OFFSET3	Not used	

CN No.	PIN No.	Signal Name	From/To	Remark
CN13	51	SP_OFFSET2	Not used	SP-711UA control
	52	SP_OFFSET1		
	53	SP_OFFSET0		
	54	GND		
	55	GND		
	56	SP_RENC	To EPI	
	57	SP_RENCZ		
	58	SP_LENC		
	59	SP_PULL		
	60	SP_LAREA		
	61	GND		
	62	GND		
	63	SP_FRQ1	To EPI	
	64	SP_FRQ0		
	65	SP_SPEED1	From EPI	
	66	SP_SPEED0		
	67	SP_UNITON*		
	68	GND		
	69	GND		
	70	VCR_VSEL1*	To DBF	VCR control
	71	VCR_VSEL0*		
	72	VCR_SM2*	From DBF	
	73	VCR_SM1*		
	74	VCR_SM0*		
	75	VCR_STOP*		
	76	VCR_FSFT*		
	77	VCR_VCNT*	To DBF	
	78	VCR_FWD/REW*	From DBF	
	79	VCR_RSTART*	To DBF	
	80	VCR_REW*	From DBF	
	81	VCR_RREW*	To DBF	
	82	VCR_FF*	From DBF	
	83	VCR_RFF*	To DBF	
	84	VCR_REC*	From DBF	
	85	VCR_RREC*	To DBF	
	86	VCR_PAUSE*	From DBF	
	87	VCR_RPAUSE*	To DBF	
	88	VCR_PLAY*	From DBF	
	89	VCR_RPLAY*	To DBF	
	90	GND		
	91	GND		
	92	COLORSHT*	From DBF	Printer shutter
	93	BWSHT*		
	94	GND		
	95	GND		
	96	EXTSYNC	Not used	TV sync
	97	GND		
	98	GND		
	99	+5.0B	From POWER	DC power(5.0V)
	100	+5.0B		

7.3 Termination of Video signals

In EUB-5500, video terminals for the monitor and printer are independent each other. Therefore, every terminal should be terminated when connecting the video device.

Section 8 Signal List

8.1 EUB-5500 Basic Unit

8.1.1 PRB PCB (PRBSW)

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	SNSRT	28C	OUT	PRB-26C	Voltage level of temperature detection for MPTEE
2	AS1	28B	OUT	AWP-26B	Voltage level of angle detection for MPTEE
3	AS2	28A	OUT	AWP-26A	Voltage level of angle detection for MPTEE
4	5VUS	28D	OUT	AWP-26D	+5V supply for MPTEE
5	DBF_PRB_D	13C	IN	DBF-113D	DBF to PRBSW serial data
6	PRB_LCK	14D	IN	DBF-111D	PRBSW I/O latch clock.
7	PRB_DBF_D	13E	OUT	DBF-114D	PRBSW to DBF serial data.
8	PRB_CK	13A	IN	DBF-112D	PRBSW I/O serial clock.
9	TRDIV_N	15A	IN	DBF-108E	Trans/Receive switch control (LVDS Negative Pole).
10	TRDIV_P	16A	IN	DBF-107E	Trans /Receive switch control (LVDS Positive Pole).
11	BCLK_N	15E	IN	DBF-110E	128ns PRBSW clock (LVDS Negative Pole). This stops at reception timing.
12	BCLK_P	16E	IN	DBF-109E	128ns PRBSW clock (LVDS Positive Pole).
13	PRB_YSYNC_N	15C	IN	CNF4-29	Y-SYNC* (LVDS Negative Pole).
14	PRB_YSYNC_P	16C	IN	CNF4-31	Y-SYNC* (LVDS Positive Pole).
15	CWEN_N	17D	IN	DBF-112E	Steering CW mode (LVDS Negative Pole)
16	CWEN_P	18D	IN	DBF-111E	Steering CW mode (LVDS Positive Pole)
17	FPGARESET*	17B	IN	CNF2-73	FPGA Reset for PRBSW.
18	SYSRESET*	18A	IN	CNF2-75	System Reset signal
19	PRBCONFDONE	18C	OUT	CNF2-31	FPGA Configuration signal
20	AD_SPARE*	23E	OUT	AWP-21E	Select signal for AD converter input. Auto-gain Control for MINI-probe is selected
21	AD_SNSRT*	24B	OUT	AWP-22B	Select signal for AD converter input. Voltage level of temperature detection for MPTEE is selected.
22	AD_ADJUST_RET*	24D	OUT	AWP-22D	Select signal for AD converter input. Auto-gain Control for ATGC PTGC is selected
23	AD_ST4V*	25A	OUT	AWP-23A	Select signal for AD converter input. ADC ref Voltage is selected.
24	AD_MP5V*	25C	OUT	AWP-23C	Select signal for AD converter input. MPTEE supply voltage is selected.

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
25	AD_ANGLE*	25E	OUT	AWP-23E	Select signal for AD converter input. Voltage level of angle detection is selected.
26	AD_0V*	26B	OUT	AWP-24B	Select signal for AD converter input. GND voltage level is selected.
27	AD_THERM*	26D	OUT	AWP-24D	Select signal for AD converter input. Voltage level of temperature detection is selected.
28	ADJCNT<1..0>	27B,27D	OUT	AWP-25B,25D	Select AD_ADJUST_RETUERN signal (PTGC ATGC voltage)
29	TDO_PRB	12B	IN	CNF3-11	JTAG Signal (Not used)
30	TCK_PRB	12C	IN	CNF3-1	JTAG Signal (Not used)
31	TDI_COM	12D	IN	CNF3-4	JTAG Signal (Not used)
32	TMS_COM	12E	IN	CNF3-2	JTAG Signal (Not used)

8.1.2 AWP PCB (PRBSW)

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	T<47..0>	58E,58C,58A,57D, 57B,56E,56C,56A, 55D,55B,54E,54C, 54A,53D,53B,52E, 52C,52A,51D,51B, 50E,50C,50A,49D, 49B,48E,48C,48A, 47D,47B,46E,46C, 46A,45D,45B,44E, 44C,44A,43D,43B, 42E,42C,42A,41D, 41B,40E,40C,40A	OUT	DBF- 23C～23A, 22E～22A, 21E～21A, 20E～20A, 19E～19A, 18E～18A, 17E～17A, 16E～16A, 15E～15A, 14E～14A	Ultrasound Transmit Signal
2	ADIN_N<47..0>	111C～111A, 108E～108A, 105E～105A, 102E～102A, 99E～99A, 96E～96A, 93E～93A, 90E～90A, 87E～87A, 84E～84A	OUT	DBF- 86B,84E,84C,84A, 82D,82B,80E,80C, 80A,78D,78B,76E, 76C,76A,74D,74B, 72E,72C,72A,70D, 70B,68E,68C,68A, 54B,52E,52C,52A, 50D,50B,48E,48C, 48A,46D,46B,44E, 44C,44A,42D,42B, 40E,40C,40A,38D, 38B,36E,36C,36A	Ultrasound Reception Signal (Differential voltage output)
3	ADIN_P<47..0>	112C～112A, 109E～109A, 106E～106A, 103E～103A, 100E～100A, 97E～97A, 94E～94A, 91E～91A, 88E～88A, 85E～85A	OUT	DBF- 87B,85E,85C,85A, 83D,83B,81E,81C, 81A,79D,79B,77E, 77C,77A,75D,75B, 73E,73C,73A,71D, 71B,69E,69C,69A, 55B,53E,53C,53A, 51D,51B,49E,49C, 49A,47D,47B,45E, 45C,45A,43D,43B, 41E,41C,41A,39D, 39B,35E,35C,35A	Ultrasound Reception Signal (Differential voltage output)
4	STCW<23..0>	37B,36E,36C,36A, 35D,35B,34E,34C, 34A,33D,33B,32E, 32C,32A,31D,31B, 30E,30C,30A,29D, 29B,28E,28C,28A	IN	CW- 11D～11A, 10E～10A, 9E～9A, 8E～8A, 7E～7A	Ultrasound transmit signal for steerable CW

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
5	STCW_N<23..0>	80D～80A, 77E～77A, 74E～74A, 71E～71A, 68E～68A	OUT	CW- 29D～29A, 26E～26A, 23E～23A, 19E～19A, 16E～16A	Steerable CW Reception signal
6	STCW_P<23..0>	81D～81A, 78E～78A, 75E～75A, 72E～72A, 69E～69A	OUT	CW- 30D～30A, 27E～27A, 24E～24A, 20E～20A, 17E～17A	Steerable CW Reception signal
7	PTGCCNT_N1	62B	IN	DBF-88D	Pre-attenuater control (10V Differential Negative Pole).
8	PTGCCNT_P1	63B	IN	DBF-89D	Pre-attenuater control (10V Differential Positive Pole)
9	ATGCCNT_N1	62D	IN	DBF-88E	Analog-TGC control (10V Differential Negative Pole). 0..-5.00V.
10	ATGCCNT_P1	63D	IN	DBF-89E	Analog-TGC control (10V Differential Positive Pole). 0.. +5.00V.
11	AD_CS*	18A	IN	DBF-109C	AD converter (Angle and thermal value for MPTEE probe convert Digital data) chip select signal
12	AD_DCLOCK	18C	IN	DBF-108C	AD converter (Angle and thermal value for MPTEE probe convert Digital data) function clock signal
13	AD_DOUT	18E	OUT	DBF-107C	AD converter (Angle and thermal value for MPTEE probe convert Digital data) data output
14	SNSRT	26C	IN	PRB-28C	Voltage level of temperature detection for MPTEE
15	AS1	32C	IN	PRB-28B	Voltage level of angle detection for MPTEE
16	AS2	35C	IN	PRB-28A	Voltage level of angle detection for MPTEE
17	5VUS	34C	OUT	PRB-28D	+5V supply for MPTEE
18	AD_SPARE*	21E	IN	PRB-23E	Select signal for AD converter input. Auto-gain Control for MINI-probe is selected
19	AD_SNSRT*	22B	IN	PRB-24B	Select signal for AD converter input. Voltage level of temperature detection for MPTEE is selected.
20	AD_ADJUST_RET*	22D	IN	PRB-24D	Select signal for AD converter input. Auto-gain Control for ATGC PTGC is selected
21	AD_ST4V*	23A	IN	PRB-25A	Select signal for AD converter input. ADC ref Voltage is selected.

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
22	AD_MP5V*	23C	IN	PRB-25C	Select signal for AD converter input. MPTEE supply voltage is selected.
23	AD_ANGLE*	23E	IN	PRB-25E	Select signal for AD converter input. Voltage level of angle detection is selected.
24	AD_0V*	24B	IN	PRB-26B	Select signal for AD converter input. GND voltage level is selected.
25	AD_THERM*	24D	IN	PRB-26D	Select signal for AD converter input. Voltage level of temperature detection is selected.
26	ADJCNY<1..0>	25B,25D	IN	PRB-27B,27D	Select AD_ADJUST_RETUERN signal (PTGC ATGC voltage)

8.1.3 DBF PCB

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	T<47..0>	23C～23A, 22E～22A, 21E～21A, 20E～20A, 19E～19A, 18E～18A, 17E～17A, 16E～16A, 15E～15A, 14E～14A	IN	PRBSW- 58E,58C,58A,57D, 57B,56E,56C,56A, 55D,55B,54E,54C, 54A,53D,53B,52E, 52C,52A,51D,51B, 50E,50C,50A,49D, 49B,48E,48C,48A, 47D,47B,46E,46C, 46A,45D,45B,44E, 44C,44A,43D,43B, 42E,42C,42A,41D, 41B,40E,40C,40A	Ultrasound transmit signal
2	ADIN_N<47..0>	86B,84E,84C,84A, 82D,82B,80E,80C, 80A,78D,78B,76E, 76C,76A,74D,74B, 72E,72C,72A,70D, 70B,68E,68C,68A, 54B,52E,52C,52A, 50D,50B,48E,48C, 48A,46D,46B,44E, 44C,44A,42D,42B, 40E,40C,40A,38D, 38B,36E,36C,36A	IN	PRBSW- 111C～111A, 108E～108A, 105E～105A, 102E～102A, 99E～99A, 96E～96A, 93E～93A, 90E～90A, 87E～87A, 84E～84A	Ultrasound Reception Signal (Differential voltage output)
3	ADIN_P<47..0>	87B,85E,85C,85A, 83D,83B,81E,81C, 81A,79D,79B,77E, 77C,77A,75D,75B, 73E,73C,73A,71D, 71B,69E,69C,69A, 55B,53E,53C,53A, 51D,51B,49E,49C, 49A,47D,47B,45E, 45C,45A,43D,43B, 41E,41C,41A,39D, 39B,35E,35C,35A	IN	PRBSW- 112C～112A, 109E～109A, 106E～106A, 103E～103A, 100E～100A, 97E～97A, 94E～94A, 91E～91A, 88E～88A, 85E～85A	Ultrasound Reception Signal (Differential voltage output)
4	USRF_I<23..0>	114A,115A,116A, 117A,118A,119A, 120A,121A,114B, 115B,116B,117B, 118B,119B,120B, 121B,114C,115C, 116C,117C,118C, 119C,120C,121C	OUT	CNF1- 1,3,5,7,9, 11,13,15,17,19, 21,23,25,27,29, 31,33,35,37,39, 41,43,45,47	Beamformed signal(I-data)
5	USRF_Q<23..0>	122A,123A,124A, 125A,126A,127A, 128A,129A,122B, 123B,124B,125B, 126B,127B,128B, 129B,122C,123C, 124C,125C,126C, 127C,128C,129C	OUT	CNF1- 49, 51,53,55,57,59, 61,63,65,67,69, 71,73,75,77,79, 81,83,85,87,89, 91,93,95	Beamformed signal(Q-data)

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
6	DBF_BEAM1*	113B	OUT	CNF1-97	Not used
7	DBF_RSTART*	113C	OUT	CNF1-99	Reception Start Signal
8	CWSYNC*	112A	OUT	CNF2-21	Not used
9	CK32ON	139C	OUT	CNF2-23	Not used
10	DBFCONFDONE	138D	OUT	CNF2-27	DBF FPGA config. Done signal
11	DMAFC<2..0>	128D,129D,129E	IN	CNF2-33,35,37	DMA function control number
12	ADJ_YSYNC*	121E	IN	CNF2-45	DBF Ysync adjustment
13	DBF_YSYNC*	122E	IN	CNF2-47	DBF Ysync
14	LCK	122D	IN	CNF2-51	Latch Clock. US Beam parameters is latced previous to Y-SYNC* assertion.
15	FFTSTART*	137C	IN	CNF2-53	FFT calculation start signal
16	CAND*	137D	IN	CNF2-55	CFM calculation start signal
17	SP_USTRIG*	118E	IN	CNF2-71	Fujinon scan timing signal
18	FPGARESET*	140C	IN	CNF2-73	FPGA reset
19	SYSRESET*	131A	IN	CNF2-75	System reset
20	TMS_COM	140E	IN	CNF3-2	JTAG TMS signal
21	TDI_COM	139E	IN	CNF3-4	JTAG TDI signal
22	TCK_DBF1	140D	IN	CNF3-5	DBF JTAG TCK signal
23	TCK_DBF2	139D	IN	CNF3-7	DBF JTAG TCK signal
24	TDO_DBF1	138E	OUT	CNF3-15	DBF JTAG TDO signal
25	TDO_DBF2	137E	OUT	CNF3-17	DBF JTAG TDO signal
26	S_STOP*	132D	OUT	CNF3-21	SPCI local bus control signal
27	S_TRDY*	132E	OUT	CNF3-23	SPCI local bus control signal
28	S_IRDY*	131D	IN	CNF3-25	SPCI local bus control signal
29	S_ERAME*	131E	IN	CNF3-27	SPCI local bus control signal
30	S_PRST*	131B	IN	CNF3-29	SPCI local bus control signal
31	S_PCLK	131C	IN	CNF3-31	SPCI local bus 30.3ns clock
32	S_CBE<1..0>*	132B,132C	IN	CNF3-33,35	SPCI local bus control signal
33	S_AD<15..0>	132A,133A,134A, 135A,133B,134B, 135B,133C,134C, 135C,133D,134D, 135D,133E,134E, 135E	IN/OUT	CNF3- 37,39,41,43,45, 47,49,51,53,55, 57,59,61,63,65, 67	SPCI local bus data signal
34	CK4F0US_P	126E	IN	CNF4-1	Transmission 4 times Reference Clock for DBF (Positive Pole)
35	CK4F0US_N	127E	IN	CNF4-3	Transmission 4 times Reference Clock for DBF (Negative Pole)
36	S_CLK_DBF_P	146B	IN	CNF4-9	SPCI clock for DBF (positive edge)
37	S_CLK_DBF_N	146A	IN	CNF4-11	SPCI clock for DBF (negative edge)
38	CK32_DBF_P	124E	IN	CNF4-15	DBF 32ns clock (positive edge)
39	CK32_DBF_N	125E	IN	CNF4-13	DBF 32ns clock (negative edge)
40	CK64DBF_P	125D	IN	CNF4-17	DBF 64ns clock (positive edge)
41	CK64DBF_N	126D	IN	CNF4-19	DBF 64ns clock (negative edge)
42	DBF_PRB_D	113D	OUT	PRB-13C	DBF to PRBSW serial data
43	PRB_LCK	111D	OUT	PRB-14D	PRBSW I/O latch clock
44	PRB_DBF_D	114D	IN	PRB-13E	PRBSW to DBF serial data
45	PRB_CK	112D	OUT	PRB-13A	PRBSW I/O serial clock
46	TRDIV_N	108E	OUT	PRB-15A	Trans/Receive switch control (LVDS Negative Pole).

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
47	TRDIV_P	107E	OUT	PRB-16A	Trans/Receive switch control (LVDS Positive Pole).
48	BCLK_N	110E	OUT	PRB-15E	128ns PRBSW clock (LVDS Negative Pole). This stops at reception timing.
49	BCLK_P	109E	OUT	PRB-16E	128ns PRBSW clock (LVDS Positive Pole).
50	CWEN_N	112E	OUT	PRB-17D	Steering CW mode (LVDS Negative Pole)
51	CWEN_P	111E	OUT	PRB-18D	Steering CW mode (LVDS Positive Pole)
52	PTGCCNT_N1	88D	OUT	AWP-62B	Pre-attenuator control (10V Differential Negative Pole)
53	PTGCCNT_P1	89D	OUT	AWP-63B	Pre-attenuator control (10V Differential Positive Pole).
54	ATGCCNT_N1	88E	OUT	AWP-62D	Analog-TGC control (10V Differential Negative Pole). 0..-5.00V.
55	ATGCCNT_P1	89E	OUT	AWP-63D	Analog-TGC control (10V Differential Positive Pole). 0.. +5.00V
56	AD_CS*	109C	OUT	AWP-18A	AD converter (Angle and thermal value for MPTEE probe convert Digital data) chip select signal
57	AD_DCLOCK	108C	OUT	AWP-18C	AD converter (Angle and thermal value for MPTEE probe convert Digital data) function clock signal
58	AD_DOUT	107C	IN	AWP-18E	AD converter (Angle and thermal value for MPTEE probe convert Digital data) data output
52	COLORSHT*	150E	OUT	CNPNL CN32-4	BW Printer Control Signal
53	BWSHT*	150D	OUT	CNPNL CN32-3	Color Printer Control Signal
54	SM2～0*	150C,150B,150A	OUT	CNPNL CN32-17, 16, 15	VCR Control Signal
55	PAUSE*	149B	OUT	CNPNL CN32-14	VCR Control Signal
56	FF*	148D	OUT	CNPNL CN32-11	VCR Control Signal
57	REW*	148E	OUT	CNPNL CN32-12	VCR Control Signal
58	STOP*	149D	OUT	CNPNL CN32-18	VCR Control Signal
59	PLAY*	149A	OUT	CNPNL CN32-13	VCR Control Signal
60	FWD/REW*	149E	OUT	CNPNL CN32-19	VCR Control Signal
61	REC*	148C	OUT	CNPNL CN32-10	VCR Control Signal
62	VCNT*	146D	OUT	CNPNL CN32-28	VCR Control Signal

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
63	FSFT*	149C	OUT	CNPNL CN32-29	VCR Control Signal
64	VSEL1,0*	148A,147E	IN	CNPNL CN32-27, 26	VCR Condition Signal
65	RREW*	147A	IN	CNPNL CN32-24	VCR Condition Signal
66	RREC*	147D	IN	CNPNL CN32-21	VCR Condition Signal
67	RFF*	147B	IN	CNPNL CN32-23	VCR Condition Signal
68	RPLAY*	147C	IN	CNPNL CN32-22	VCR Condition Signal
69	VCRRSTART*	146C	IN	CNPNL CN32-20	VCR Condition Signal
70	RPAUSE*	146E	IN	CNPNL CN32-14	VCR Condition Signal
71	T_CWS<23..0>	29D～29A, 28E～28A, 27E～27A, 26E～26A, 25E～25A	OUT	CW- 5D～5A, 4E～4A, 3E～3A, 2E～2A, 1E～1A	Steerable CW Transmission Signal
72	DBF-CW-D	109D	OUT	CW-94D	Control data (serial)
73	CW_CK	108D	OUT	CW-91D	Clock for control data
74	CW_LCK	107D	OUT	CW-94E	Clock to set control data
75	CW-DBF-D	110D	IN	CW-105C	CW version Data(serial)
76	STCWEN-N	114D	OUT	CW-102D	Steering CW mode control.
77	STCWEN-P	113D	OUT	CW-103D	Steering CW mode control.
78	SP_USTRIG	116E	OUT		Fujinon trigger signal
79	SP_USTRIG_GND	117E	IN/OUT		GND for SP_USTRIG
80	SP_AMODE	118D	IN		Fujinon Input
81	SP_AMODE_GND	119D	IN/OUT		GND for SP_AMODE
82	SP_GAIN	116D	OUT		Gain curve for Fujinon Input
83	SP_GAIN_GND	117D	IN/OUT		GND for SP_GAIN
84	MB_VER<7..0>	140B-137B, 140A-137A	IN	MB-	Mother Board Version signal
85	STVC<4..0>	111A-107A	OUT	CN3-10,9,3,2,1	Voltage control signal for Steerable CW transmission.
86	DFRQ1,0	110C,110B	IN	CND6-14,15	PEN-CW connection status
87	EPRB1,0	108B,107B	IN	CND6-12,13	PEN-CW connection status
88	ETRIN	109B	IN	CND6-16	PEN-CW connection status

8.1.4 EPI PCB

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	USRF_I<23..0>	CNF1- 1,3,5,7,9, 11,13,15,17,19, 21,23,25,27,29, 31,33,35,37,39, 41,43,45,47	IN	DBF- 114A,115A,116A, 117A,118A,119A, 120A,121A,114B, 115B,116B,117B, 118B,119B,120B, 121B,114C,115C, 116C,117C,118C, 119C,120C,121C, CW- 108A,108B,108C, 108D,108E,109A, 109B,109C,109D, 109E,110A,110B, 110C,110D,110E, 111A	Beamformed Signal(I-Data)
2	USRF_Q<23..0>	CNF1- 49, 51,53,55,57,59, 61,63,65,67,69, 71,73,75,77,79, 81,83,85,87,89, 91,93,95	IN	DBF- 122A,123A,124A, 125A,126A,127A, 128A,129A,122B, 123B,124B,125B, 126B,127B,128B, 129B,122C,123C, 124C,125C,126C, 127C,128C,129C CW- 111B,111C,111D, 111E,112A,112B, 112C,112D,112E, 113A,113B,113C, 113D,113E,114A, 114B	Beamformed Signal(Q-Data)
3	DBF_BEAM1*	CNF1-97	IN	DBF-113B	Not Used
4	DBF_RSTART*	CNF1-99	IN	DBF-113C	Reception Start Signal
5	HFRZ	CNF2-1	IN	CN80-1	Freeze On Signal by Hardware
6	SP_RENCZ	CNF2-3	IN	CN8-44	Fujinon Sync Signal
7	SP_RENC	CNF2-5	IN	CN8-45	Fujinon Sync Signal
8	SP_FREQ<1..0>	CNF2-7,9	IN	CN8-37,38	Fujinon Freq Select Signal
9	SP_UNITON*	CNF2-11	IN	CN8-34	Fujinon Unit Connect Signal
10	RSYNC	CNF2-15	IN	BIO-20A	ECG R Side Sync Signal
11	LSYNC	CNF2-17	IN	BIO-20B	ECG L Side Sync Signal
12	R-TRIG	CNF2-19	IN	BIO-10B, CN80-2	ECG R-Trig Signal
13	CWSYNC*	CNF2-21	IN	DBF-112A, CW-103E	Not Used
14	CK32ON	CNF2-23	IN	DBF-139C	Not Used
15	BIOCONFDONE	CNF2-25	IN	BIO-4B	BIO FPGA Config. Done Signal
16	DBFCONFDONE	CNF2-27	IN	DBF-138D	DBF FPGA Config. Done Signal
17	CWCONFDONE	CNF2-29	IN	CW-103A	CW FPGA Config. Done Signal
18	PRBCONFDONE	CNF2-31	IN	PRB-18C	PRB FPGA Config. Done Signal
19	DMAFC<2..0>	CNF2-33,35,37	OUT	DBF- 128D,129D129E	DMA Function Control number
20	BIO_SDATA	CNF2-39	IN/OUT	BIO-4A	BIO Serial I/F Data Signal
21	BIO_CS*	CNF2-41	OUT	BIO-7B	BIO Serial I/F CS* Signal
22	BIO_YSYNC*	CNF2-43	OUT	BIO-10D	BIO Ysync

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
23	ADJ_YSYNC*	CNF2-45	OUT	DBF-121E	DBF_Ysync Adjustment
24	DBF_YSYNC*	CNF2-47	OUT	DBF-122E	DBF Ysync
25	YSYNC*	CNF2-49	OUT	NC	Ysync
26	LCK	CNF2-51	OUT	DBF-122D	Latch Clock. US Beam parameters I latched previous to Y-SYNC* assertion.
27	FFTSTART*	CNF2-53	OUT	DBF-137C	FFT Calculation Start Signal
28	CNAD*	CNF2-55	OUT	DBF-137D	CFM Calculation Start Signal
29	SYNCERR	CNF2-63	OUT	CN80-3	Sync Error Signal
30	SP_SPEED<1..0>	CNF2-65,67	OUT	CN8-35,36	Fujinon Probe Rotation Speed
31	SP_USTRIG*	CNF2-71	OUT	DBF-118E	Fujinon Scan Timing Signal
32	FPGARESET*	CNF2-73	OUT	PRB-17B, DBF-140C, BIO-26B, CW-100A	FPGA Reset. FPGA Configuration begins after FPGARESET* positive edge.
33	SYSRESET*	CNF2-75	OUT	PRB-18A, DBF-131A, BIO-23B, CW-100B, CN80-4	System Reset. Asserted at Power On and Software Boot.
34	PWSW_KB	CNF2-77	OUT	CN80-7	Power Off Interruption to EUB Software through KBIF.
35	STBY	CNF2-79	IN	CN51-1, JP10-2	Stand-by Switch Signal.
36	STBY-	CNF2-80	IN	CN51-2, JP11-2	Stand-by Switch Signal.
36	TMS_COM	CNF3-2	OUT	PRB-12E, DBF-140E, CW-103B, BIO-17A	JTAG TMS Signal
37	TDI_COM	CNF3-4	OUT	PRB-12D, DBF-139E, CW-102B, BIO-15A	JTAG TDI Signal
38	TCK_PRB	CNF3-1	OUT	PRB-12C	PRB JTAG TCK Signal
39	TCK_CW	CNF3-3	OUT	CW-105B	CW JTAG TCK Signal
40	TCK_DBF1	CNF3-5	OUT	DBF-140D	DBF JTAG TCK Signal
41	TCK_DBF2	CNF3-7	OUT	DBF-139D	DBF JTAG TCK Signal
42	TCK_BIO	CNF3-9	OUT	BIO-17B	BIO JTAG TCK Signal
43	TDO_PRB	CNF3-11	IN	PRB-12B	PRB JTAG TDO Signal
44	TDO_CW	CNF3-13	IN	CW-104B	CW JTAG TDO Signal
45	TDO_DBF1	CNF3-15	IN	DBF-138E	DBF JTAG TDO Signal
46	TDO_DBF2	CNF3-17	IN	DBF-137E	DBF JTAG TDO Signal
47	TDO_BIO	CNF3-19	IN	BIO-15B	BIO JTAG TDO Signal
48	S_STOP*	CNF3-21	IN	DBF-132D, BIO-23A	S-PCI Local Bus Control Signal
49	S_TRDY*	CNF3-23	IN	DBF-132E, BIO-25A	S-PCI Local Bus Control Signal
50	S_IRDY*	CNF3-25	OUT	DBF-131D, BIO-27A	S-PCI Local Bus Control Signal
51	S_FRAME*	CNF3-27	OUT	DBF-131E, BIO-29A	S-PCI Local Bus Control Signal
52	S_PRST*	CNF3-29	OUT	DBF-131B, BIO-35A	S-PCI Local Bus Control Signal
53	S_PCLK	CNF3-31	OUT	DBF-131C, BIO-37A	S-PCI Local Bus 30.3ns(33MHz) Clock

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
54	S_CBE<1..0>*	CNF3-33,35	OUT	DBF-132B,132C, BIO-31A,33A	S-PCI Local Bus Control Signal
55	S_AD<15..0>	CNF3-37,39,41,43,45,47,49,51,53,55,57,59,61,63,65,67	IN/OUT	DBF-132A,133A,134A,135A,133B,134B,135B,133C,134C,135C,133D,134D,135D,133E,134E,135E BIO-23C,24C,25C,26C,27C,28C,29C,30C,31C,32C,33C,34C,35C,36C,37C,38C	S-PCI Local Bus Data Signal
56	TCICLK	CNF6-1	OUT	MAP1,2-CNF6-1	TCI Bus 40ns(25MHz) Clock
57	TCISYNC	CNF6-3	OUT	MAP1,2-CNF6-3	TCI Bus Sync Signal
58	TCIEN	CNF6-5	OUT	MAP1,2-CNF6-5	TCI Bus Enable Signal
59	TCIERR*	CNF6-7	OUT	MAP1,2-CNF6-7	TCI Bus Error Signal
60	TCIDA<7..0>	CNF6-9,11,13,15,17,19,21,23	OUT	MAP1,2-CNF6-9,11,13,15,17,19,21,23	TCI Bus Data Signal (I-Data)
61	TCIDB<7..0>	CNF6-25,27,29,31,33,35,37,39	OUT	MAP1,2-CNF6-25,27,29,31,33,35,37,39	TCI Bus Data Signal (Q-Data)
62	IIS_SDATA	CNF6-43	IN	MAP1,2-CNF6-43	IIS Audio Serial Data Signal
63	IIS_LRCK	CNF6-45	IN	MAP1,2-CNF6-45	IIS Audio LR Indicate Signal
64	IIS_SCLK	CNF6-47	IN	MAP1,2-CNF6-47	IIS Audio Sampling Clock
65	IIS_MCLK	CNF6-49	IN	MAP1,2-CNF6-49	IIS Audio Master Clock
66	TCK_MAP1	CNF6-10	OUT	MAP1,2-CNF6-10	MAP1 JTAG TCK Signal
67	TCK_MAP2	CNF6-14	OUT	MAP1,2-CNF6-14	MAP2 JTAG TCK Signal
68	TDO_MAP1	CNF6-18	IN	MAP1,2-CNF6-18	MAP1 JTAG TDO Signal
69	TDO_MAP2	CNF6-22	IN	MAP1,2-CNF6-22	MAP2 JTAG TDO Signal
70	TMS_COM	CNF6-26	OUT	MAP1,2-CNF6-26	MAP1,2 JTAG TMS Signal
71	TDI_COM	CNF6-30	OUT	MAP1,2-CNF6-30	MAP1,2 JTAG TDI Signal
72	CK4FOUS_P	CNF4-1	OUT	DBF-126E	Transmission 4 times Reference Clock for DBF (Positive Pole)
73	CK4FOUS_N	CNF4-3	OUT	DBF-127E	Transmission 4 times Reference Clock for DBF (Negative Pole)
74	CK4FOCW_P	CNF4-7	OUT	CW-105A	Transmission 4 times Reference Clock for CW (Positive Pole)
75	CK4FOCW_N	CNF4-5	OUT	CW-104A	Transmission 4 times Reference Clock for CW (Negative Pole)
76	S_CLK_DBF_P	CNF4-9	OUT	DBF-146B	S-PCI Clock for DBF (Positive Pole)
77	S_CLK_DBF_N	CNF4-11	OUT	DBF-146A	S-PCI Clock for DBF (Negative Pole)
78	S_CLK_BIO_P	CNF4-25	OUT	BIO-15E	S-PCI Clock for BIO (Positive Pole)
79	S_CLK_BIO_N	CNF4-27	OUT	BIO-16E	S-PCI Clock for BIO (Negative Pole)
80	CK32DBF_P	CNF4-15	OUT	DBF-124E	DBF 31.2MHz (32nS) Clock (Positive Pole)
81	CK32DBF_N	CNF4-13	OUT	DBF-125E	DBF 31.2MHz (32nS) Clock (Negative Pole)
82	CK64DBF_P	CNF4-17	OUT	DBF-125D	DBF 15.6MHz (64nS) Clock. (Positive Pole)

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
83	CK64DBF_N	CNF4-19	OUT	DBF-126D	DBF 15.6MHz (64nS) Clock. (Negative Pole)
84	CK64BIO_P	CNF4-23	OUT	BIO-15D	BIO 15.6MHz (64nS) Clock. (Positive Pole)
85	CK64BIO_N	CNF4-21	OUT	BIO-16D	BIO 15.6MHz (64nS) Clock. (Negative Pole)
86	PRB_YSYNC_P	CNF4-31	OUT	PRB-16C	PRB YSYNC* (Positive Pole)
87	PRB_YSYNC_N	CNF4-29	OUT	PRB-15C	PRB YSYNC* (Negative Pole)
88	CWADCLK_P	CNF4-39	OUT	CW-114D	CW AD Clock (Positive Pole)
89	CWADCLK_N	CNF4-37	OUT	CW-114E	CW AD Clock (Negative Pole)
90	RPWSW+	CNF7-1	OUT	PCMB-	PCMB Power-On signal.
91	RPWSW-	CNF7-2	IN	PCMB-	PCMB Power-On signal.
92	SOUND_REC1	CNF5-1	OUT	CN8-95	Sound Signal to VCR
93	SOUND_REC2	CNF5-3	OUT	CN8-94	Sound Signal to VCR
94	SOUND_VCR1	CNF5-7	IN	CN8-91	Sound Signal from VCR
95	SOUND_VCR2	CNF5-9	IN	CN8-90	Sound Signal from VCR
96	SOUND_SP1	CNF5-15	OUT	CNS1-1	Sound Signal to Speaker
97	SOUND_SP2	CNF5-13	OUT	CNS2-1	Sound Signal to Speaker
98	AD<31..0>	J1- B20,A20,B21,A22, B23,A23,B24,A25, B27,A28,B29,A29, B30,A31,B32,A32, A44,B45,A46,B47, A47,B48,A49,B52, B53,A54,B55,A55, B56,A57,B58,A58	IN/OUT	PCMB-	PCI Bus Data Signal
99	CBE<3..0>*	J1- B26,B33,B44,A52	IN/OUT	PCMB-	PCI Bus Control Signal
100	RST*	J1-A15	IN	PCMB-	PCI Bus Control Signal
101	CLK	J1-B16	IN	PCMB-	PCI Bus 30.3ns(33MHz) Clock
102	IDSEL	J1-A26	IN	PCMB-	PCI Bus Control Signal
103	FRAME*	J1-A34	IN/OUT	PCMB-	PCI Bus Control Signal
104	IRDY*	J1-B35	IN/OUT	PCMB-	PCI Bus Control Signal
105	DEVSEL*	J1-B37	IN/OUT	PCMB-	PCI Bus Control Signal
106	TRDY*	J1-A36	IN/OUT	PCMB-	PCI Bus Control Signal
107	STOP*	J1-A38	IN/OUT	PCMB-	PCI Bus Control Signal
108	PAR	J1-A43	IN/OUT	PCMB-	PCI Bus Control Signal
109	REQ*	J1-B18	OUT	PCMB-	PCI Bus Control Signal
110	GNT*	J1-A17	IN	PCMB-	PCI Bus Control Signal
111	INTA*	J1-A6	OUT	PCMB-	PCI Bus Control Signal
112	PRSNT1*	J1-B9	OUT	PCMB-	PCI Bus Control Signal
113	PRSNT2*	J1-B11	OUT	PCMB-	PCI Bus Control Signal
114	PERR*	J1-B40	OUT	PCMB-	PCI Bus Control Signal
115	SERR*	J1-B42	IN/OUT	PCMB-	PCI Bus Control Signal

8.1.5 MAP PCB

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	TCICLK	CNF6-1	IN	EPI-CNF6-1	TCI Bus 40ns(25MHz) Clock
2	TCISYNC	CNF6-3	IN	EPI-CNF6-3	TCI Bus Sync Signal
3	TCIEN	CNF6-5	IN	EPI-CNF6-5	TCI Bus Enable Signal
4	TCIERR*	CNF6-7	IN	EPI-CNF6-7	TCI Bus Error Signal
5	TCIDA<7..0>	CNF6- 9,11,13,15, 17,19,21,23	IN	EPI-CNF6- 9,11,13,15, 17,19,21,23	TCI Bus Data Signal (I-Data)
6	TCIDB<7..0>	CNF6- 25,27,29,31, 33,35,37,39	IN	EPI-CNF6- 25,27,29,31, 33,35,37,39	TCI Bus Data Signal (Q-Data)
7	IIS_SDATA	CNF6-43	OUT	EPI-CNF6-43	IIS Audio Serial Data Signal
8	IIS_LRCK	CNF6-45	OUT	EPI-CNF6-45	IIS Audio LR Indicate Signal
9	IIS_SCLK	CNF6-47	OUT	EPI-CNF6-47	IIS Audio Sampling Clock
10	IIS_MCLK	CNF6-49	OUT	EPI-CNF6-49	IIS Audio Master Clock
11	TCK_MAP1	CNF6-10	IN	EPI-CNF6-10	MAP1 JTAG TCK Signal
12	TCK_MAP2	CNF6-14	IN	EPI-CNF6-14	MAP2 JTAG TCK Signal
13	TDO_MAP1	CNF6-18	OUT	EPI-CNF6-18	MAP1 JTAG TDO Signal
14	TDO_MAP2	CNF6-22	OUT	EPI-CNF6-22	MAP2 JTAG TDO Signal
15	TMS_COM	CNF6-26	IN	EPI-CNF6-26	MAP1,2 JTAG TMS Signal
16	TDI_COM	CNF6-30	IN	EPI-CNF6-30	MAP1,2 JTAG TDI Signal

8.2 BIO Unit EZU-EK25

8.2.1 BIO PCB

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	SCK_BIO_N	16E	IN	CNF4-27	Spci Clock
2	SCK_BIO_P	15E	IN	CNF4-25	Spci Clock
3	S_AD15～1	23C,24C,25C,26C, 27C,28C,29C,30C, 31C,32C,33C,34C, 35C,36C,37C,38C	IN/OUT	CNF3- 37,39,41,43,45,47, 49,51,53,55,57,59, 61,63,65,67	Spci Address Data bus.
4	S_CBE<1..0>	31A,33A	IN	CNF3-33,35	Byte Enable
5	S_FRME*	29A	IN	CNF3-27	Spci Cycle Frame
6	S_IRDY*	27A	IN	CNF3-25	Spci Initiator Ready
7	S_TRDY*	25A	OUT	CNF3-23	Spci Target Ready
8	S_STOP*	23A	OUT	CNF3-21	Spci Stop
9	S_PRST*	35A	IN	CNF3-29	Spci Reset
10	SYNC1	20B	IN	CNF2-17	ECG SYNC1 signal
11	SYNC2	20A	IN	CNF2-15	ECG SYNC2 signal
12	64NS_N	16D	IN	CNF4-21	15.6MHz (64nS) System Clock.
13	64NS_P	15D	IN	CNF4-23	15.6MHz (64nS) System Clock.
14	FPGARESET*	26B	IN	CNF2-73	FPGA reset. FPGA configuration begins after FPGARESET* positive edge.
15	BIOCONFDONE	4B	OUT	CNF2-25	FPGA configuration
16	R-TRIG	10B	OUT	CN80-2,CNF2-19	ECG R-Wave Trig Signal
17	BIO_CS*	7B	IN	CNF2-41	Time Stamp Chip Select
18	BIO_Sdata	4A	IN	CNF2-39	Time Stamp Serial Data
19	TMS_COM	17A	IN	CNF3-2	JTAG Test Mode Selector
20	TDI_COM	15A	IN	CNF3-4	JTAG Test Data input
21	TCK_BIO	17B	IN	CNF3-9	JTAG Test Clock
22	TDO_BIO	15B	OUT	CNF3-19	JTAG Test Data output

8.3 CW Unit EZU-ST5,EZU-CW4

8.3.1 CW PCB

No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
1	T_CWS<23..0>	5D～5A, 4E～4A, 3E～3A, 2E～2A, 1E～1A	IN	DBF-29D～29A, 28E～28A, 27E～27A, 26E～26A, 25E～25A	Steerable CW Transmission input Signal
2	STCW<23..0>	11D～11A, 10E～10A, 9E～9A, 8E～8A, 7E～7A	OUT	AWP-37B, 36E, 36C, 36A, 35D, 35B, 34E, 34C, 34A, 33D, 33B, 32E, 32C, 32A, 31D, 31B, 30E, 30C, 30A, 29D, 29B, 28E, 28C, 28A	Steerable CW Transmission output Signal
3	STCW-N<23..0>	29D～29A, 26E～26A, 23E～23A, 19E～19A, 16E～16A	IN	AWP-80D～80A, 77E～77A, 74E～74A, 71E～71A, 68E～68A	Steerable CW Reception Signal
4	STCW-P<23..0>	30D～30A, 27E～27A, 24E～24A, 20E～20A, 17E～17A	IN	AWP-81D～81A, 78E～78A, 75E～75A, 72E～72A, 69E～69A	Steerable CW Reception Signal
5	USRF-I<15..0>	111A, 110E～110A, 109E～109A, 108E～108A	OUT	EPI-CNF1-31, 29, 27, 25, 23, 21, 19, 17, 15, 13, 11, 9, 7, 5, 3, 1	CW A/D Output Signal
6	USRF-Q<15..0>	114B～114A, 113E～113A, 112E～112A, 111E～111B	OUT	EPI-CNF1-79, 77, 75, 73, 71, 69, 67, 65, 63, 61, 59, 57, 55, 53, 51, 49	CW A/D Output Signal
7	CWADCLK_N	114E	IN	EPI-CNF4-37	CW A/D clock.
8	CWADCLK_P	114D	IN	EPI-CNF4-39	CW A/D clock.
9	CK4FOCW-N	104A	IN	EPI-CNF4-5	4 times reference clock for CWREC (LVDS Negative pole).
10	CK4FOCW-P	105A	IN	EPI-CNF4-7	4 times reference clock for CWREC (LVDS Positive pole).
11	DBF-CW-D	94D	IN	DBF-109D	Control data (serial)
12	CW_CK	91D	IN	DBF-108D	Clock for control data
13	CW_LCK	94E	IN	DBF-107D	Clock to set control data
14	CW-DBF-D	105C	OUT	DBF-110D	CW version Data(serial)
15	STCWEN-N	102D	IN	DBF-114D	Steering CW mode control.
16	STCWEN-P	103D	IN	DBF-113D	Steering CW mode control.
17	CWCONFDONE	103A	OUT	EPI-CNF2-29	FPGA config completion data
18	SYSRESET*	100B	IN	EPI-CNF2-75	System Reset. Asserted at power on and software boot.
19	FPGARESET*	100A	IN	EPI-CNF2-73	FPGA reset. FPGA configuration begins after FPGARESET* positive edge.

20	CWSYNC*	103E	IN	EPI-CNF2-21	Not used.
No.	Signal Name	Terminal No.	IN/OUT	From/To	Description
21	TCK_CW	105B	IN	EPI-CNF3-3	Not used.
22	TDO_CW	104B	IN	EPI-CNF3-13	Not used.
23	TMS_COM	103B	IN	EPI-CNF3-2	Not used.
24	TDI_COM	102B	IN	EPI-CNF3-4	Not used.

Section 9 Maintenance

9.1 Fan Filter

Every day	Once a week	Once a month	Others

Clean the dust-proof air filter at the air inlet of power unit located at the bottom front of equipment. If the filter is choked, the breaker may be cut off or the power unit may possibly be damaged.

NOTE:
- Be sure to turn OFF the power before cleaning the filter.
- Never turn ON the power unless mounting the filter. Dust around the power unit may enter into it causing a fire.

9.2 Other Maintenance Items

1. Probe

Every day	Once a week	Once a month	Others

(1) After using the equipment, use any tissue or soft cloth to completely wipe off jelly stuck to the probe.

(2) When wiping off the probe, do not use hard paper or cloth.

(3) Put the probe in the probe holder or probe case, and keep it carefully.

(4) Care should be taken not to give strong shock to the probe or drop it.

2. Control Panel

Every day	Once a week	Once a month	Others

(1) After using the equipment, turn OFF the power and completely wipe off jelly stuck to the surface of control panel.

3. System Cabinet

Every day	**Once a week**	Once a month	Others

(1) Before cleaning the system cabinet, turn OFF the power and extract the power cable from the power outlet.

(2) Use cloth moistened with a neutral detergent to remove stains, and then wipe off it with soft dry cloth.

NOTE:
- Never use organic solvent such as thinner.
- Care should be taken for any liquid such as a detergent not to directly drop on the equipment.
- When cleaning the equipment, care should be taken no to drop any liquid on the inside of equipment, probe, probe connector or control panel.

4. Monitor

Every day	Once a week	Once a month	Others

(1) Before cleaning the monitor, turn OFF the power to the main unit and extract the power cable from the power outlet.

(2) Use cloth supplemented to the equipment to clean the surface of monitor. Use soft cloth and glass cleaner to wipe off any sticky stains. Use cloth moistened with a neutral detergent to clean the top and side faces of monitor cover, and then wipe off them with soft cloth.

NOTE:
- Never use organic solvent such as thinner.
- Care should be taken for any liquid such as a detergent not to directly drop on the equipment.
- Do not use a glass cleaner made of hydrocarbon.

5. VCR

Every day	Once a week	Once a month	Others

(1) Before cleaning VCR, turn OFF the power to the main unit and extract the power cable from the power outlet.

(2) Use dry cloth to clean the surface of VCR. Use soft cloth and glass cleaner to wipe off any sticky stains. Do not use moistened cloth or detergent.

(3) Follow the instruction manual provided by the manufacturer to clean the record/ playback head with the head cleaner specified. For details, refer to the instruction manual of VCR.

6. Video Printer

Every day	Once a week	Once a month	Others

(1) Before cleaning the video printer, turn OFF the power to the main unit and extract the power cable from the power outlet.

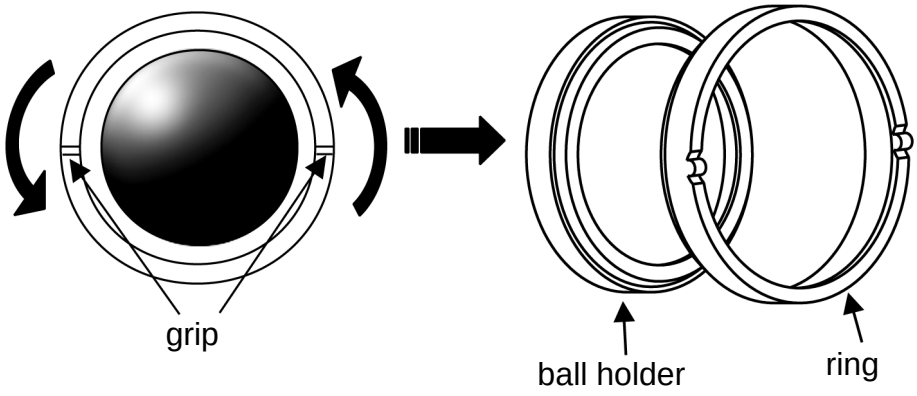
(2) Use dry cloth to clean the surface of video printer. Use soft cloth and glass cleaner to wipe off any sticky stains. Do not use moistened cloth or detergent.

(3) Put the cleaning sheet supplemented to the device, which is specified by the printer manufacturer, through the printer head to clean it. For details, refer to the instruction manual of the video printer.

7. Cleaning of the trackball

Every day	Once a week	Once a month	Others

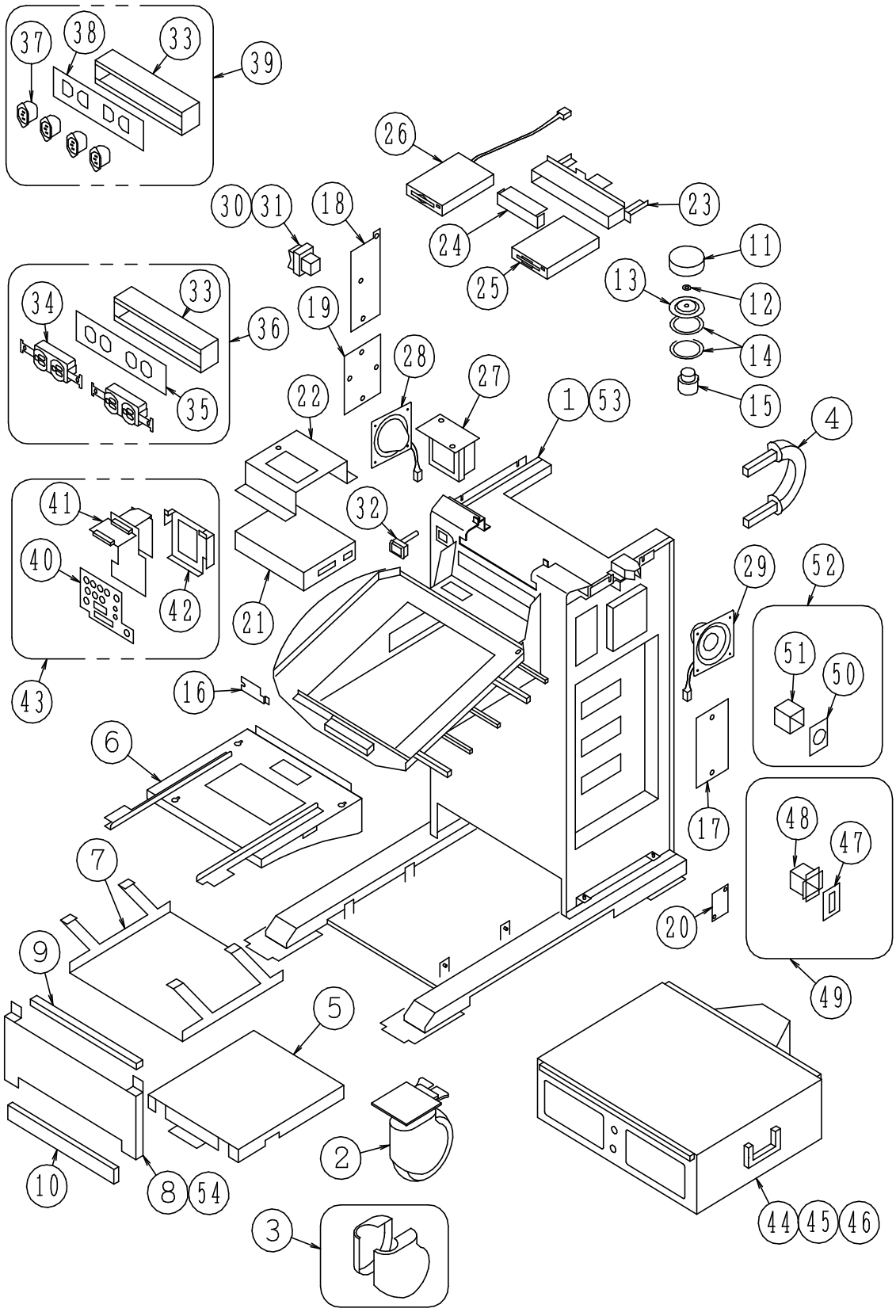
- Before you clean the trackball, turn off the unit and unplug the power cable from the outlet.
- Do not use wet cloth or detergent. If it gets into the trackball unit, it may cause damage.
- You can clean the track ball by turning the ring around the ball to remove the ring, ball holder, and ball from the trackball unit.
  If the ball does not roll smoothly because of dust inside the trackball, use dry, soft cloth to remove the dust.



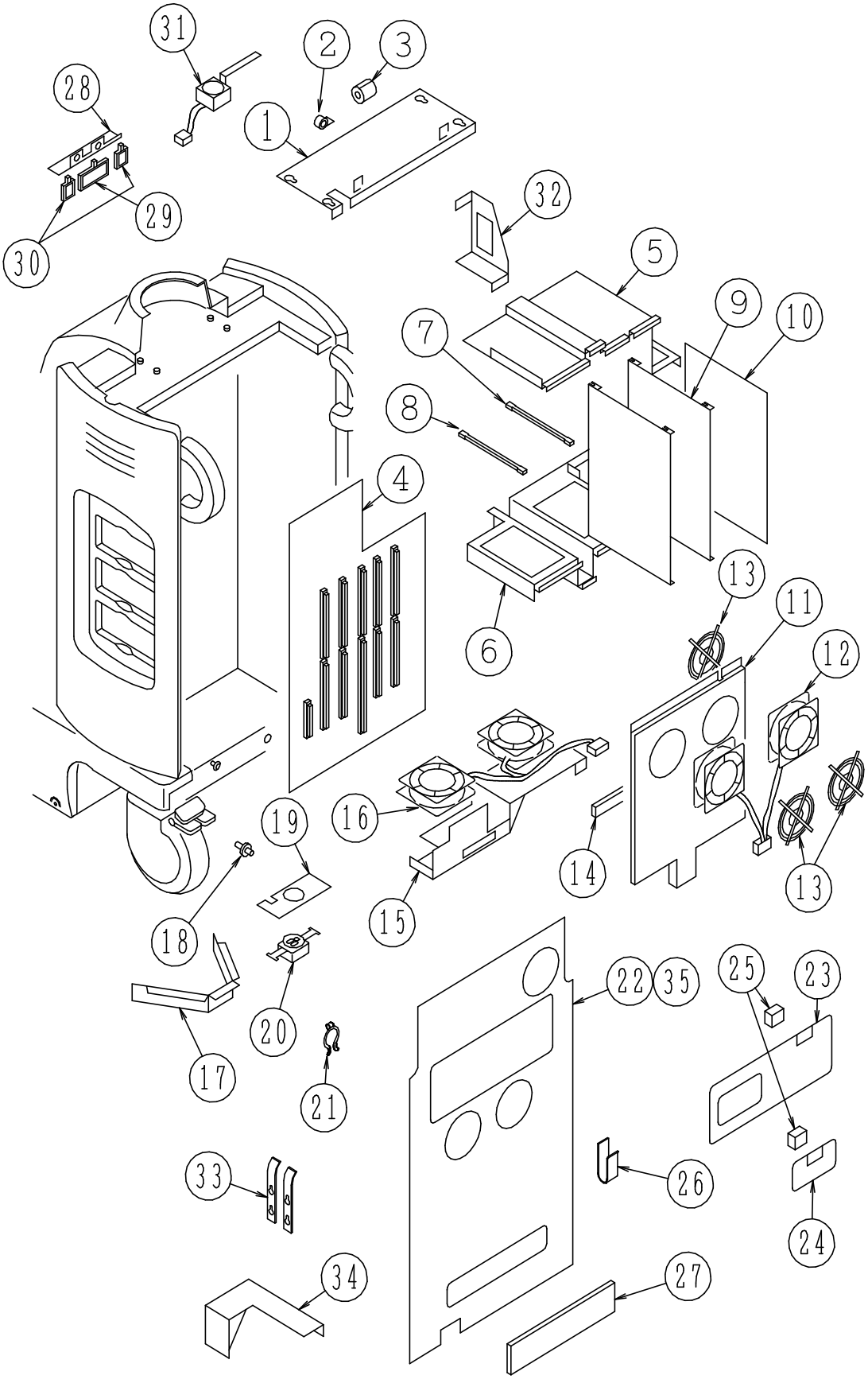
Cleaning of the trackball

Section 10 Parts List

1. CART1



2. CART2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2. CART2

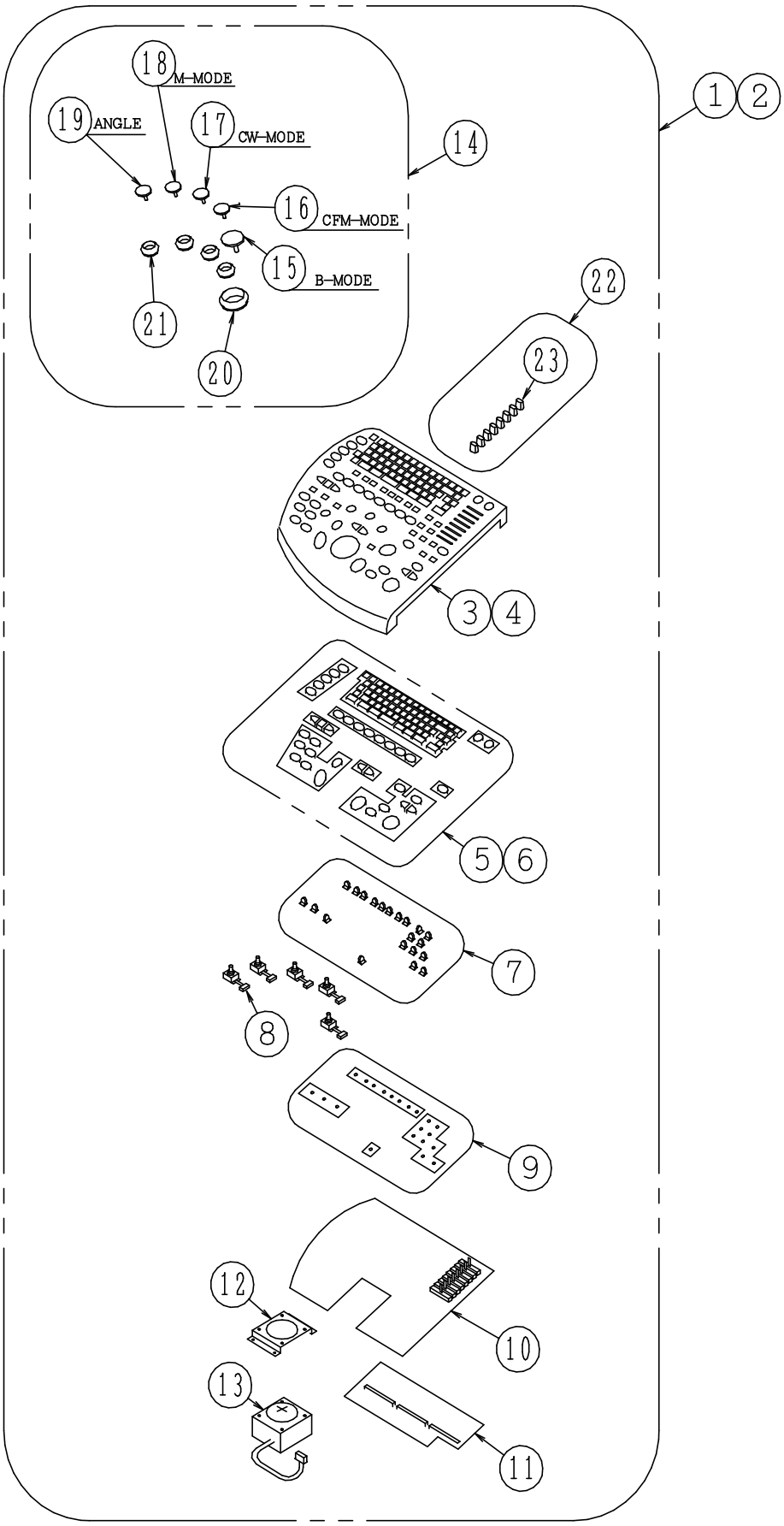
KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
1	7319017A	TOP SHEILED/6500		1	
2	J839A106	FG CLAMP/6500		1	
3	7319215E	CORE/6500		1	
4	7511408A	MB PCB/5500		1	
5	7321641A	TOP SHASSIS/5500		1	
6	7312642A	BTM SHASSIS/5500		1	
7	1481564B	GUIDE 3.5MM		2	for DBF
8	J8991105	GUIDE 50-6030		10	
9	7416598A	SLD PLATE/6500		2	
10	7418415A	SLD PLATE/5500		1	
11	7323765A	PCB COVER/5500		1	
12	7416827A	PCB FAN SET/6500		1	
13	1475231A	FAN NET/6500		3	
14	7418420A	PCB RUBBER/5500		1	
15	7323766A	BTM FAN PLT/5500		1	
16	7418571A	BTM FAN SET/5500		1	
17	7416604A	PS COVER/6500		1	
18	J836A048	GND TERMINAL		1	
19	7416602A	MT PANEL/6500		1	
20	J8320206	OUTLET 8210-I		1	
21	J839A124	CABLE CLIP		1	
22	7218757A	REAR COVER/5500		1	
23	7419805A	REAR PLT A/5500		1	
24	7419806A	REAR PLT B/5500		1	
25	7415785A	REAR SPONGE/6500		2	
26	2455033A	CORD HOLDER		1	
27	7415786A	AIR FILTER/6500		1	
28	7420761A	CLAMP PLATE/5500		1	
29	7420762A	CLAMP A		1	
30	7420763B	CLAMP B		2	
31	7419925A	MAP FAN UNIT/5500		1	
32	7420909A	HD BASE/5500		1	
33	7419583A	PCB GUIDE/5500		2	
34	7415963A	PRB BTM SPT/6500		1	
35	7218943A	R-COVER/5500USA		1	USA

1. CART1

KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
1	7218905A	CART/5500		1	
2	7312175B	CASTER/6500		4	
3	7324997B	CASTER COVER		4	
4	7415673B	HANDLE/5500		2	
5	7319012A	VCR BASE/6500		1	
6	7319011A	OP-PLATE/6500		1	
7	7319019A	TRAY/6500		1	
8	7416594C	CN-COVER/5500		1	
9	7415783A	F-SPONGE A/6500		1	
10	7415784A	F-SPONGE B/6500		1	
11	1434754A	ADJUSTING KNOB		1	
12	1427110A	SLIDING PLATE B		1	
13	144095XA	KNOB WASHER		1	
14	1416371A	SLIDING PLATE A		2	
15	1469374A	HANGER BASE/6500		1	
16	7416607C	F-BLIND PLT/5500		1	
17	7418412A	BLIND PLT A/5500		1	
18	7418413A	BLIND PLT B/5500		1	
19	7413414A	BLIND PLT C/5500		1	
20	7418417A	ECG BLIND/5500		2	
21	7324030A	CD-RW UNIT		1	
22	7419818A	CD-R PLATE/5500		1	
23	7323332A	FD PLATE/5500		1	
24	7419616A	MOD BLIND/5500		1	
25	7315074A	FD UNIT		1	
26	UoF324	EZU-MO1		1	
27	7419924A	KB FAN UNIT/5500		1	
28	7418574A	SP-CABLE L/5500		1	
29	7415755A	SP-CABLE R/5500		1	
30	K214A116	BRKER 100V/6500		1	100V
31	K214A117	BRKER 230V/6500		1	230V
32	7317898A	SW-CABLE/6500		1	
33	7416601A	OUT-PNL SLD/6500		1	
34	J8310801	OUTLET 8200-I		2	100V
35	7416599A	OUT-PNL(N)/6500		1	100V

KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
36	7319731A	OUTLET(N)/6500		1	100V
37	J8310501	OUTLET NC-183C		4	230V
38	7416600A	OUT-PNL(E)/6500		1	230V
39	7319732A	OUTLET(E)/6500		1	230V
40	7319018A	CN-PANEL/6500		1	
41	7510161A	CN-PCB/5500		1	
42	7419749A	CN-SHIELD/5500		1	
43	7420022A	CN-PNL UNIT/5500		1	
44	7216682A	P.S. HM-071C		1	100V
45	7216682B	P.S. HM-071CE		1	230V
46	7319377B	P.S. HM-071C		1	120V
47	7418968A	ECG PANEL/EK25		1	EZU-EK25
48	7419966A	ECG SLD/EK25		1	EZU-EK25
49	7419720A	ECG BOX/EK25		1	EZU-EK25
50	7416610C	CW PANEL/5500		1	
51	7416611A	CW SHIELD/6500		1	
52	7417170C	CW UNIT/5500		1	
53	7218940A	CART/5500USA		1	USA
54	7417919B	CN-COVER/5500USA		1	USA

3. KEYBOARD


18
M-MODE
19
ANGLE
17
CW-MODE
14
1
2
16
CFM-MODE
15
B-MODE
21
20
22
23
3
4
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12
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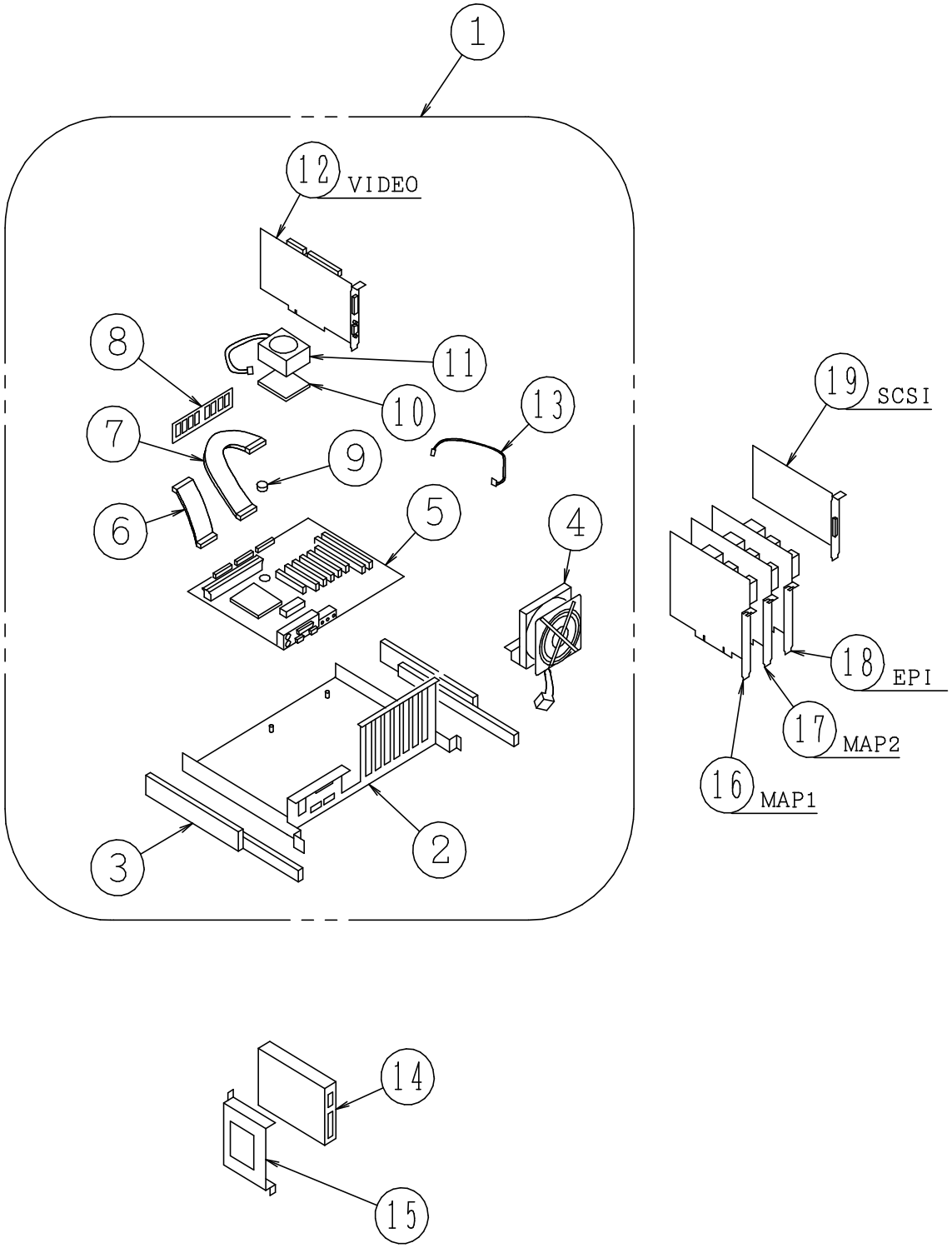
13
11

3. KEYBOARD

KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
1	7319385F	KEYBOARD UNIT(E)		1	ENGLISH
2	7319385G	KEYBOARD UNIT(F)		1	FRANCH
3	7320775B	KB COVER(E)		1	ENGLISH
4	7320775C	KB COVER(F)		1	FRANCH
5	7320775W	RUBBER KEY SET-E		1	ENGLISH
6	7320775Y	RUBBER KEY SET-F		1	FRANCH
7	7320775L	PADDLE SET		1	
8	7320775M	ENCORDER		5	
9	7320775N	PDL RUBBER SET		1	
10	7320775P	KB PCB		1	
11	7320775Q	KBIF PCB		1	
12	7320775R	TB PLATE		1	
13	7320775T	LIGHT TRACK BALL		1	
14	7320775D	KNOB SET		1	
15	7323484A	B GAIN CAP		1	
16	7323484B	CFA GAIN CAP		1	
17	7323484C	CW GAIN CAP		1	
18	7323484D	M GAIN CAP		1	
19	7323484E	ANGLE CAP		1	
20	7323484F	B GAIN KNOB		1	
21	7323484G	GAIN KNOB		4	
22	7320775F	VOL KNOB SET		1	
23	7420871A	VOL KNOB		8	

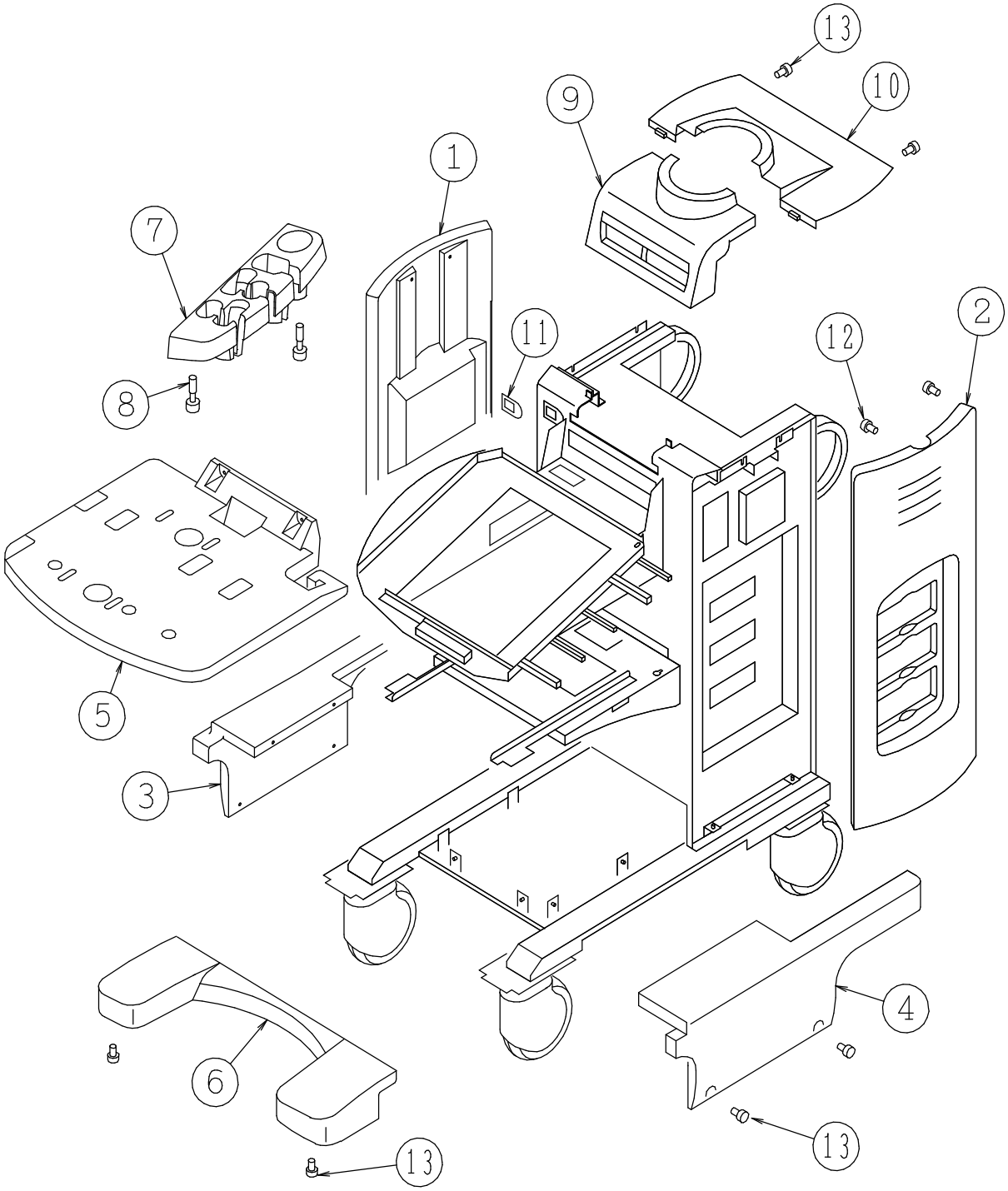
4. PC UNIT



4. PC UNIT

KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
1	7218910A	PC UNIT/5500		1	w/o HDD
2	7218756A	PC RACK/5500		1	
3	7416847A	PC RAIL/6500		2	
4	7419926A	PC FAN UNIT/5500		1	
5	7323252 B	PCMB/8500		1	
6	7413124A	FD CABLE		1	
7	7413123A	HD CABLE		1	
8	7319181A	MEMORY PCB		1	
9	K641A005	PCMB BATTERY		1	
10	7413437C	CPU2		1	
11	7325076A	CPU FAN		1	
12	7419573A	VIDEO PCB		1	
13	7418573A	CN69 CABLE/5500		1	
14	7412262A	HD UNIT(NL)		1	
15	7420908A	HD PLATE/5500		1	
16	7511277A	MAP1 PCB/5500		1	
17	7511277B	MAP2 PCB/5500		1	
18	7511275A	EPI PCB/5500		1	
19	7315726A	SCSI BRD/PI1		1	EZU-PI1

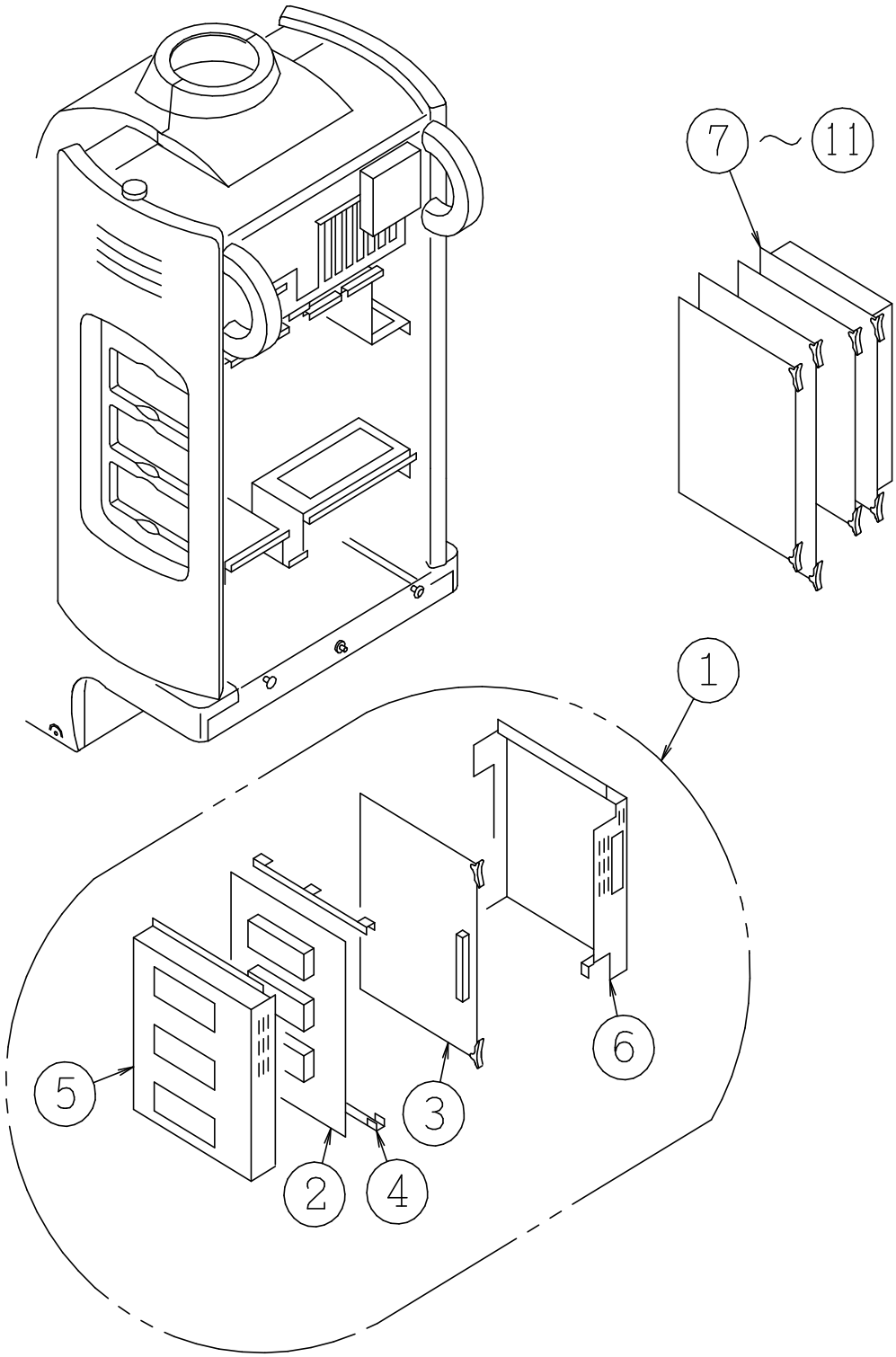
5. COVER



5. COVER

KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
1	7112095A	S-COVER L/6500		1	
2	7112096A	S-COVER R/6500		1	
3	7112097A	B-COVER L/6500		1	
4	7112098A	B-COVER R/6500		1	
5	7112099B	OPTION BASE/5500		1	
6	7112100A	BUMPER/6500		1	
7	7111880A	PRB HOLDER/6500		1	
8	L931A049	HOLDER KNOB/6500		2	
9	7215817D	F-COVER/5500		1	
10	7215818C	TOP COVER/5500		1	
11	7415788A	SW LABEL/6500		1	
12	7417225A	UREA SCREW L=6		4	
13	7417225C	UREA SCREW L=10		8	

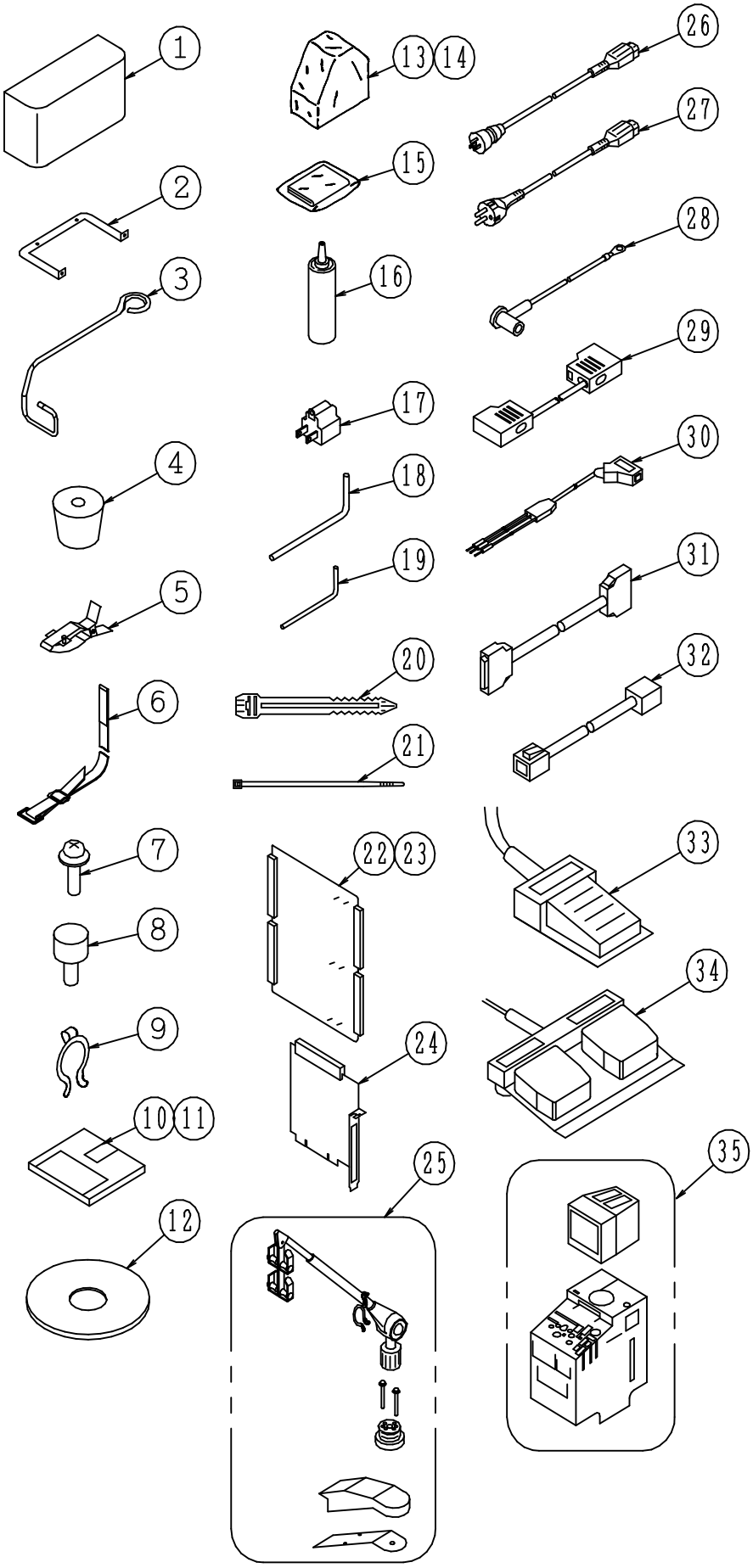
6. PCB



6. PCB

KEY NO.	PARTS NO.	PART NAME		QTY	REMARKS
1	7323170A	PRB-SW UNIT/5500		1	
2	7511409A	PRB PCB/6500		1	
3	7511410A	AWP PCB/5500		1	
4	7418408A	PRB PLATE/5500		2	
5	7323183A	PRB SHLD F/5500		1	
6	7321646A	PRB SHLD R/5500		1	
7	UoF281	EZU-ST5		1	
8	UoF320	EZU-CW4		1	
9	7511411A	DBF PCB/5500		1	
10	7511406A	BIO PCB/EK25		1	EZU-EK25
11	7319339A	POWER PCB/5500		1	

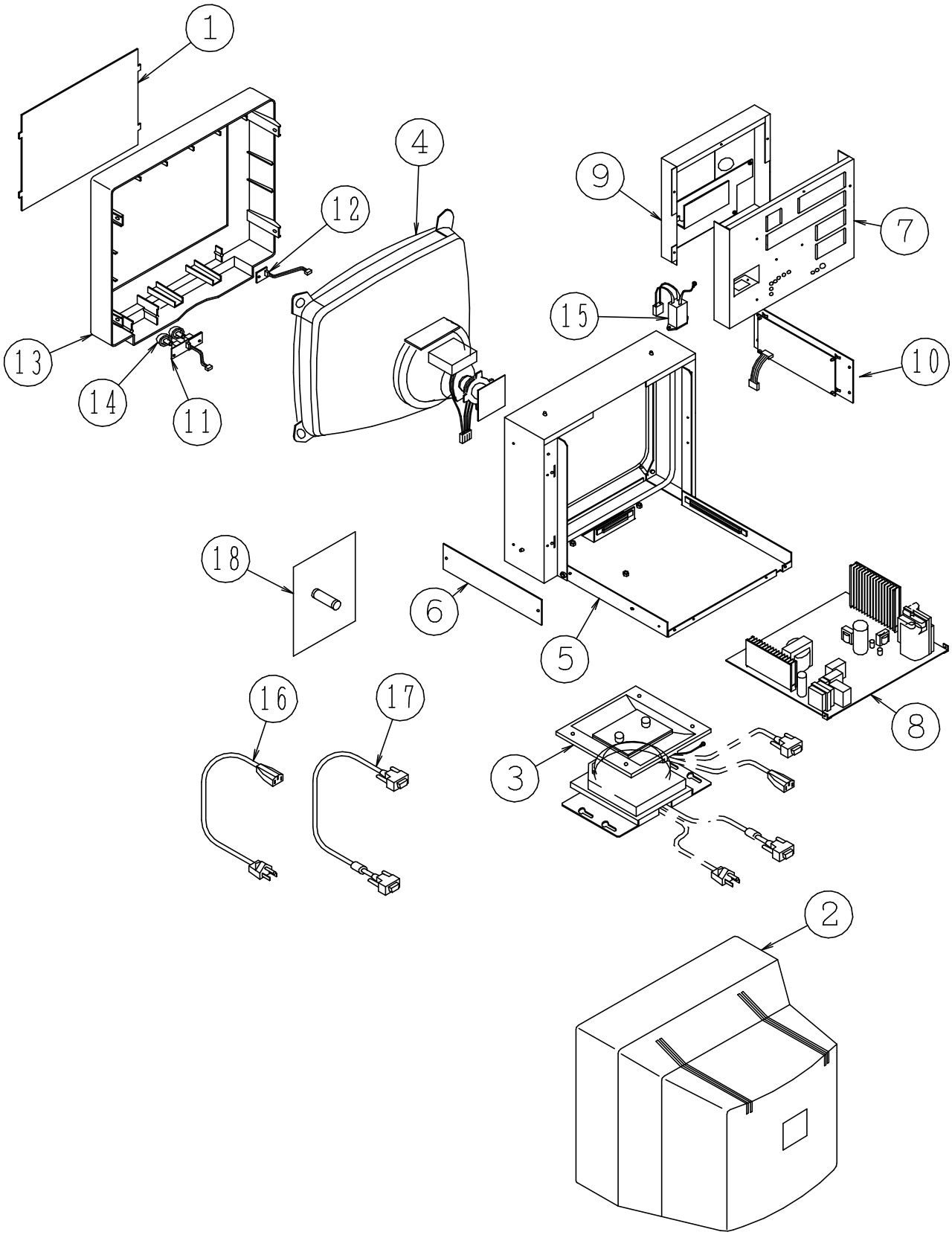
7. ACCESSORIES



7. ACCESSORIES

KEY No.	PARTS NO.	PART NAME		QTY	REMARKS
1	7416612A	VCR CASE/6500		1	
2	7416613A	CASE PLATE/6500		1	
3	1384039B	PRB HANGER/6500		1	
4	7421322A	RUBBER FOOT/5500		4	
5	J8611101	ECG CLIP		1	EZU-EK25
6	S290A007	BELT/6500		6	
7	M6450316	M3 SCREW		4	
8	7417225A	UREA SCREW L=6		4	
9	J839A124	CABLE CLIP		4	
10	1469554B	MO DISK (230MB)		1	
11	7412783A	MO DISK (640MB)		1	
12	J749A019	CD-RW DISK		1	
13	13777XXF	DUST COVER		1	
14	13777XXD	DUST COVER		1	USA
15	7313483U	CLOTH FOR CRT		1	
16	S2909001	ULTRASOUND JELLY		2	
17	J8329001	2P-3P ADAPTER		1	
18	N3100406	SOCKET SCREW(M6)		1	
19	N3100404	SOCKET SCREW(M4)		1	
20	J8390813	COAD BAND		5	
21	J8390755	CABLE TIE		10	
22	7326351A	CU EXTIN.BOARD/5500		1	
23	7326351B	DBF EXTIN.BOARD/5500		1	for DBF
24	7326351C	PCI EXTIN.BOARD/5500		1	for MAP,EPI
25	UOF197	EZU-TH4		1	
26	E910A037	POWER CORD		1	100/120V
27	E910A038	POWER CORD		1	230V
28	1477344A	EARTH CORD		1	
29	UoF907	EZU-RO1		1	
30	7324262A	ECG CABLE		1	EZU-EK25
31	7315798A	SCSI CABLE/Pi1		1	EZU-Pi1
32	7414389A	LAN CABLE/Pi2		1	EZU-Pi6
33	UoF582	EZU-FS1		1	
34	UoF230	EZU-FS2		1	
35	7419321A	V-COVER/65-5500		1	VINYL COVER, NOT USA

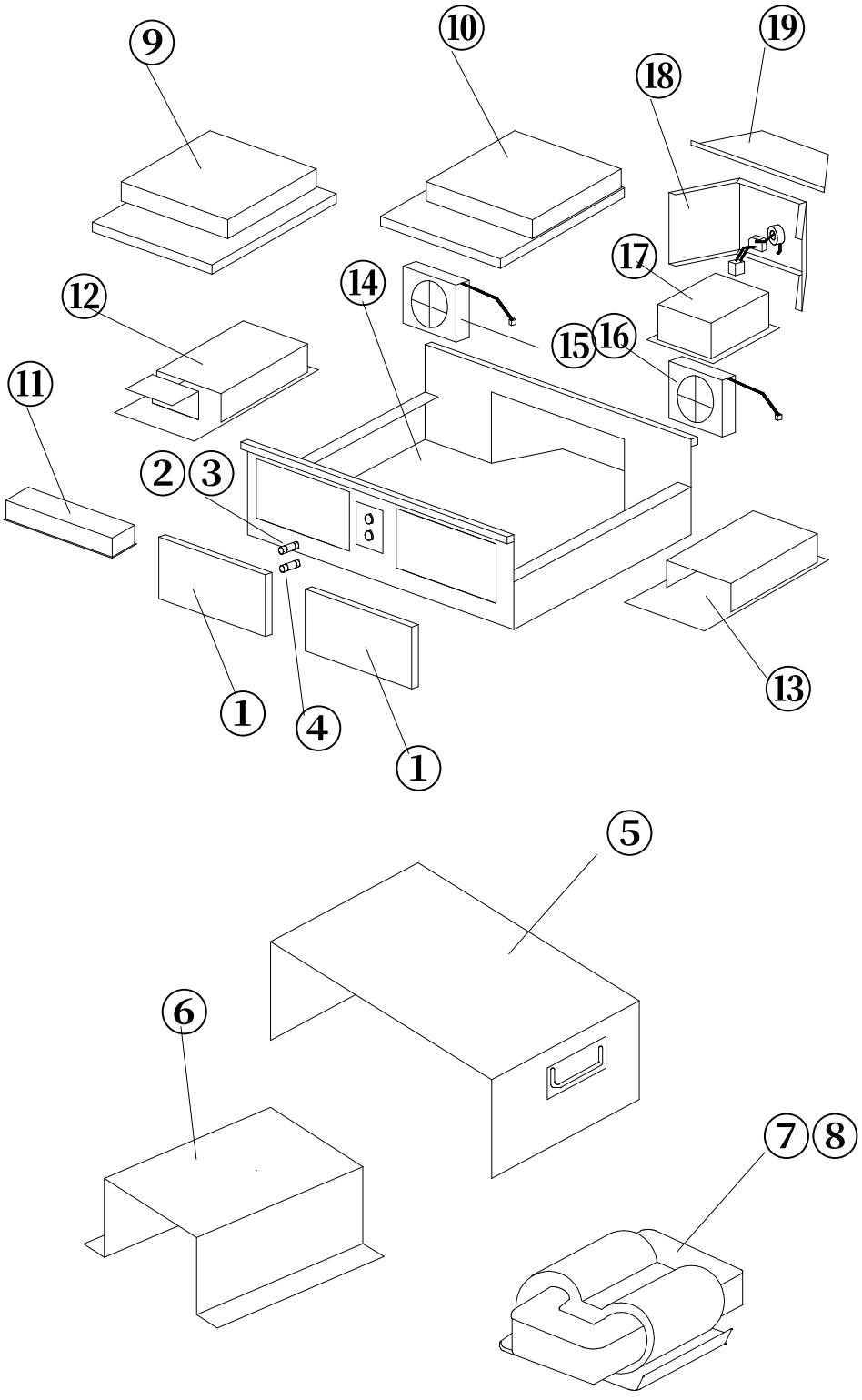
8. MONITOR



8. MONITOR

KEY NO.	PARTS NO.	PART NAME		QTY	REMARKS
1	7313483N	FILTER/MT24		1	
2	7313483B	B-CVR/MT24		1	
3	7313483C	TILT/MT24		1	
4	7313483D	CRT/MT24		1	
5	7313483E	BASE/MT24		1	
6	7313483F	SIDE/MT24		1	
7	7313483G	FTG/MT24		1	
8	7313483H	MAIN BOARD/MT24		1	
9	7321445A	VIDEO BRD/MT24-1		1	
10	7313483K	CONT BRD/MT24		1	
11	7321445B	VR BOARD/MT24-1		1	
12	7313483M	LED BOARD/MT24		1	
13	7313483V	BEZEL/MT24		1	
14	7313483P	KNOB/MT24		1	
15	7313483Q	AC FILTER/MT24		1	
16	7313483R	AC CABLE/MT24		1	
17	7313483S	SIGNAL/MT24		1	
18	7313483T	FUSE/MT24		1	

9. POWER SUPPLY



9. POWER SUPPLY

KEY NO.	PARTS NO.	PART NAME		QTY	REMARKS
1	7320729A	FILTER /071C		1	
2	7320729B	FUSE 6.3A/250V		1	100V
3	7320729C	FUSE 3.15A/250V		1	230V
4	7320729D	FUSE 1.6A/250V		1	
5	7320729E	BONNET/071C		1	
6	7320729F	SHIELD PLT/071C		1	
7	7320729G	TRANSFOMER/07C		1	100~120V
8	7320729H	TRANSFOMER/07C		1	220~240V
9	7320729J	A-LV PCB/071C		1	
10	7320729K	A-HV PCB/071C		1	
11	7320729L	SUB-PS BD/071C		1	
12	7320729M	MC-DC PCB/071C		1	
13	7320729N	MC-AC PCB/071C		1	
14	7320729P	SHASSIS/071C		1	
15	7320729Q	FAN L ASSY/071C		1	
16	7320729R	FAN R ASSY/071C		1	
17	7320729S	FILTER PCB/071C		1	
18	7320729T	CN-CASE/071C		1	
19	7320729U	CN-COVER/071C		1	